Dan

MODEL 7040

PCM SPAN—REPEATER TEST SET

SERVICE

Northeast Electronics Instruction Manual
A7040-00-601 Issue 1A August 1980

northeast electronics
DIVISION OF tau-tron inc.
A UNIT OF GENERAL SIGNAL

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Regional Drive
P.O. Box 2021
Concord, NH 03301

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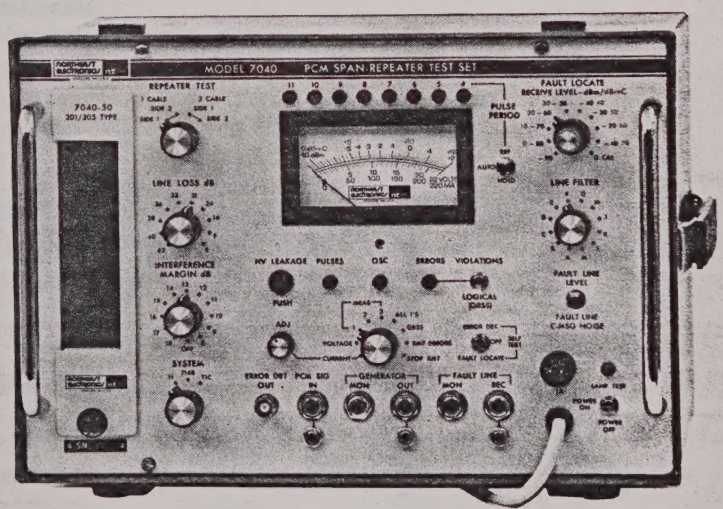

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ADDENDUM NO. 2
November 1982

	PAGE
Repeater Inserts 7040-51 and 7040-53 Design Change	AD2–1/AD2–2

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FIGURE	TITLE	PAGE
AD2–1	7040-51 Repeater Insert Schematic Diagram	AD2–1/AD2–2
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ADDENDUM NO. 2
November 1982
MODEL 7040 PCM SPAN-REPEATER TEST SET
A7040-00-601 ISSUE 1A

AD2.1 A design change has been made to Repeater Inserts 7040-51 and 7040-53. The change enables the test set to monitor a line repeater that has separate fault locating lines. If you have the earlier version of either of these repeater inserts, then the design change can easily be implemented in the field by adding a strap as shown in the revised Figures 6—34 and 6—36 below. The change is only required if the line repeaters under test have separate fault locating lines.

AD2.2 Make the following changes to the manual.

a. Paragraph 5.12, step 11 . . . change "See Figure 5—2." to read "See Figure 5—1."

b. Paragraph 5.14, step 5 . . . add "Function switch to ALL 1's".

AD2.3 Later versions of the 7040-51 repeater insert have a permanently installed switch illustrated below. This switch is clearly labeled "dual (shorted)" and "single (open)" to indicate the direction switch must be in for separate (dual) or single fault locating lines, respectively.

AD2.4 This addendum incorporates all previous addendums to this issue.

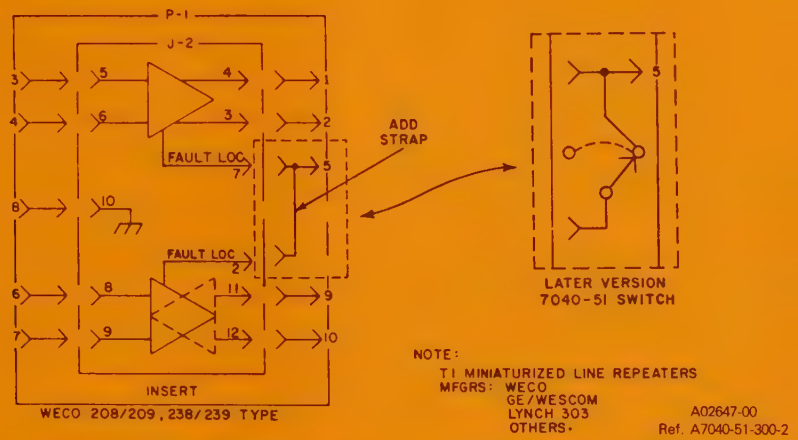

Figure AD2—1. 7040-51 Repeater Insert Schematic Diagram (See Figure 6—34, Page 6—38).

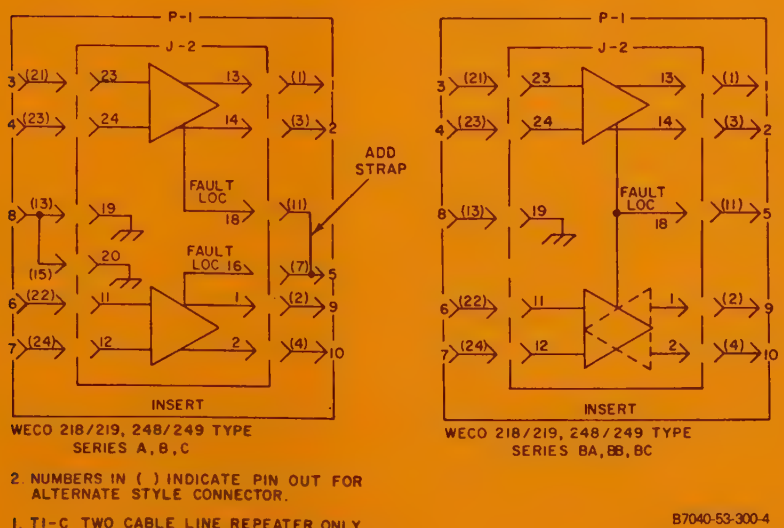

Figure AD2—2. 7040-53 Repeater Insert Schematic Diagram (See Figure 6—36, Page 6—39).

SECTION 1

GENERAL DESCRIPTION

1.1 The Northeast Electronics Model 7040 is designed for central office testing/troubleshooting of PCM span lines and individual PCM repeaters. The 7040 is equipped with the features needed for:

- ☐ Span line fault locating;
- ☐ Span line performance testing . . . on an end-to-end or loop-back basis;
- ☐ Office and line repeater pre-installation/merit testing.

1.2 The 7040 has selectable send/receive bit rates compatible with T1 (1.544 Mb/s), T148 (2.37 Mb/s), and T1C (3.152 Mb/s) PCM systems.

1.3 TRANSMIT CAPABILITIES

1.4 The Model 7040 generates the five most frequently needed test signal pulse patterns: QRSS (quasi-random) . . . ALL 1's (1111) . . . MEASURE 1, 2, and 3. The QRSS and ALL 1's patterns are typically required by span line and repeater performance test practices. The QRSS pattern is a standard quasi-random word format that accurately simulates the signals normally present in working PCM lines. The ALL 1's pattern has a pulse in every time slot.

1.5 The 7040 can transmit the QRSS pattern as an error-free signal, or as a signal into which errors have been deliberately introduced for convenient marking (identification) of a particular PCM line. When QRSS is used to test individual repeaters, the 7040 can insert known amounts of interfering signal to determine near-end-crosstalk (NEXT) and signal-to-noise (S/N) marginal limits.

1.6 The MEASURE 1, 2, and 3 pulse patterns are typically required by span line fault locating practices and by individual repeater test practices. MEASURE 1 exercises both positive and negative pulse regeneration capabilities of repeaters. MEASURE 2 and 3 help isolate repeater problems by allowing separate checking of positive and negative pulse regeneration capabilities.

1.7 The MEASURE 1, 2, and 3 pulse patterns can be "modulated" by any of 12 standard audio frequencies (A thru M) associated with the fault locating filters at repeater points along a span line. This permits selective identification of trouble sections on a line.

1.8 With the Model 7040, any of the 12 frequencies can be quickly and accurately selected by a single switch. No "fine tuning" is required for either send or receive.

1.9 Decreasing the pulse period (increasing density) of the MEASURE 1, 2, or 3 patterns can be used to place greater operating stress on repeaters. This helps to identify marginal repeaters and other obscure troubles. With the Model 7040, pulse period can be stepped from: (a) 1 pulse group every 11 time slots, to (b) 1 pulse group every 4 time slots. The stepping can be either manual or automatic. The automatic stepping is particularly convenient when gathering data for obscure trouble analysis charts defined in various span line fault locating practices.

1.10 RECEIVE CAPABILITIES

1.11 When performing span line fault locating tests, the Model 7040 measures the level (in dBm) of the audio interrogation tone received from a fault locating pair. The measured level is displayed on a front panel meter.

1.12 A C-message noise measuring feature is also built into the 7040 for convenience in evaluating fault locating line noise, as required by many fault locating practices. Noise values (in dBrnC) are displayed on the front panel meter. A separate noise measuring set is not needed.

1.13 The 7040 is also equipped for monitoring active PCM lines carrying live traffic or test signals. It detects and indicates presence of: pulses, bipolar violation errors (T1/T1C), disparity errors (T148), 10-kHz line oscillations, and ALL 1's (1111) line oscillations. (The deliberate bipolar violations present in a T148 ternary-coded signal are ignored.)

1.14 In addition, the 7040 can detect and indicate any logical bit errors introduced into a QRSS test signal by PCM spans, repeaters, or other equipment. It performs 100-percent, bit-by-bit checking on the QRSS signal generated by its own transmitter or any other QRSS source such as the Northeast Electronics Model 7046. This capability is a helpful diagnostic tool, and can be particularly significant when evaluating PCM lines used for data service.

1.15 ADDITIONAL CAPABILITIES

1.16 Adapter accessories allow the 7040 to test individual office and line repeaters of many types produced by many different manufacturers. The 7040 supplies correct dc power to the repeater under test and allows independent testing of repeater sides 1 and 2.

A built-in artificial line with selectable attenuation simulates normal cable losses and other characteristics seen by the repeater in actual service. An HV leakage test is built-in for checking insulation/isolation of the repeater powering circuits from earth (case) ground.

1.17 For verification of operational performance, the 7040 design incorporates self check and lamp test capabilities.

1.18 APPLICATIONS

1.19 The following paragraphs briefly describe the capabilities of the Model 7040 when used in different applications.

1.20 SPAN LINE FAULT LOCATING

1.21 MEASURE 1, 2, and 3 pulse patterns are selectable for fault locating purposes. The selected MEASURE pattern can be "modulated" by any one of 12 standard audio frequencies (coded A through M) associated with the fault locating filters at repeater points along a span line. This permits selective identification of trouble sections on a span line.

1.22 The Model 7040 accurately measures the level of each audio interrogation frequency (A through M) received from a fault locating pair associated with the span line being tested. The measured level is displayed on a front panel meter. The level can be displayed as either: (1) the absolute (calibrated) level being received, or (2) a plus/minus deviation from a user-set reference level.

1.23 While interrogating a span line, varying degrees of stress can be placed on repeaters in the line by increasing pulse density (decreasing pulse period) of the MEASURE signal pattern. This is accomplished by cycling through pulse periods 11 to 4. Cycling can be either automatic or manual. Calibration of the 7040 audio frequency level measurement circuits is automatically corrected to compensate for the test pattern power changes that occur when stepping pulse periods.

1.24 A C-message noise measurement feature is also built into the 7040 for convenient evaluation of noise on fault locating pairs, as required by many fault locating practices. A separate noise measuring set is not required when using the Model 7040.

1.25 SPAN LINE PERFORMANCE TESTING

1.26 Normally the first test performed on a suspected faulty span is a PCM transmission performance test. This determines whether the span line is, or is not, the actual cause of a reported trouble. When two 7040's are used, one sends a signal over the line and the other monitors the line for errors and oscillations. Or, a single 7040 can perform both the send and receive functions on a loop-back basis.

1.27 The signal pattern normally used for span line performance testing is the Bell System standard QRSS pattern. This is a quasi-random word pattern consisting of 1,048,575 bits with a maximum of 14 successive zeros to simulate average traffic density. The 14 consecutive zeros stress the clock recovery circuits in the repeaters. Deliberate errors can be introduced into the bit stream for identifying a particular span line at the receiving end.

1.28 The 7040 also allows selection of an ALL 1's test signal pattern which is easier for repeaters to handle than is the QRSS pattern.

1.29 Span line performance is evaluated by observing a set of front panel indicator lamps. The line can be checked for the presence of pulses, nominal 10 kHz oscillations, bipolar violations and "All 1's" on T1 and T1C lines, and disparity errors on T148 lines. In addition, further checking can be accomplished by analyzing, on a bit-by-bit basis (logical error detection), a QRSS signal applied to the span line.

1.30 INDIVIDUAL REPEATER TESTING

1.31 The 7040 allows testing of office and line repeaters before installation or before committing the repeaters to repair. Several available repeater well adapters serve repeaters from several manufacturers.

1.32 Independent testing of side 1 and side 2 for both 1-cable (bidirectional) repeaters and for 2-cable (unidirectional) line repeaters is switch selectable. The repeater under test is supplied with a constant current that can be adjusted within the range of 50 to 220 milliamperes. Both the operating current and the voltage across the repeater can be monitored on the 7040 front panel meter. An insulation resistance check is made by applying 200 Vdc between the powering ground lead and the case. Leakage is indicated when the associated indicator lamp is lighted.

1.33 The repeater can be tested using the QRSS, ALL 1's, or MEASURE 1, 2, or 3 signals. The output of the repeater can be monitored for pulses, oscillations, and errors by use of the indicator lamps. A switch selectable artificial line in the 7040 simulates various lengths of actual line to test the repeater under realistic operating conditions. Operating margin against interference (NEXT) (signal-to-noise ratio) is tested by adding

varying amounts of interference to a normal signal until errors are observed. The NEXT selection range covers 18 to 8 dB below the level of an ALL 1's signal at the repeater input.

1.34 A good overall evaluation of a repeater can be obtained by merit testing. This consists of applying the MEAS 1 fault locating signal to the repeater and then cycling through pulse periods 11 through 4. Meter readings are recorded and compared against limits to determine the operational condition of the repeater.

SECTION 2

SPECIFICATIONS

2.1 This section lists major specifications for the Model 7040 PCM Span-Repeater Test Set.

Table 2—1. Model 7040 Specifications

TRANSMITTER	
Bit Rates	
T1:	1.544 Mb/s ± 0.005%.
T148:	2.37 Mb/s ± 0.005%.
T1C:	3.152 Mb/s ± 0.005%.
Time Slots	
T1:	648 nsec.
T148:	422 nsec.
T1C:	317 nsec.
Pulse Widths	
T1:	324 nsec ± 10%.
T148:	211 nsec ± 10%.
T1C:	160 nsec ± 10%.
Unbalance:	less than ± 5%.
Max. Rise/Fall Times	
T1:	80 nsec.
T148:	50 nsec.
T1C:	30 nsec.
Pulse Amplitude:	3V ± 10%, base to peak.
Trailing Edge Overshoot:	10 to 30% of pulse amplitude.
Output Impedance:	100 ohms ± 10%, balanced.
Selectable Pulse Patterns	
MEAS 1:	Groups of positive and negative pulse trios that alternate at the selected audio rate.

Table 2—1. (Cont'd)

TRANSMITTER (Cont'd)

MEAS 2:	Groups of positive pulse trios and normal bipolar pulses that alternate at the selected audio rate.
MEAS 3:	Groups of negative pulse trios and normal bipolar pulses that alternate at the selected audio rate.
ALL 1's:	A logical 1 pulse is present in each time slot.
QRSS:	The standard Bell System quasi-random signal source format. The word length is 1,048,575 bits with no more than 14 successive zeros in the T1 signal. The bit stream can be either error-free or can contain deliberate errors at the rate of one every ⅔ of a second. There is no zero suppression for T1C signal.
Fault Locating Frequencies:	A = 832 Hz, B = 928 Hz, C = 1048 Hz, D = 1206 Hz, E = 1340 Hz, F = 1508 Hz, G = 1722 Hz, H = 2008 Hz, J = 2193 Hz, K = 2413 Hz, L = 2680 Hz, M = 3017 Hz
Fault Locate Freq. Tolerance:	All ± 0.5%.
Pulse Periods:	11 to 4 selectable manually or automatically. In automatic mode, steps from pulse period 11 to pulse period 4, stopping at each pulse period for approximately 5 seconds.
Generator Monitor Jack Impedance:	430-ohm resistors in series with the tip and the ring.

RECEIVER

Fault Locating Parameters:	
Receive Level Measure Sensitivity:	−90 to 0 dBm full scale in 10-dB steps.
Vernier Range:	15 dB.
C-Message Noise Range:	0 to 70 dBrnC full scale in 10-dB steps.
Level Reading Accuracy:	± 1 dB at 0 dB on meter; ± 2 dB at −10 dB on meter.
Frequencies Detectable:	Same as transmitter, filter selectivity of 1 ± 1 Hz centered at selected frequency.
Input Impedance:	900 ohms ± 10%, balanced.
Common Mode Rejection:	60 dB min at 4 kHz.
Fault Line Monitor Jack Impedance:	10 kohms.

Table 2—1. (Cont'd)

RECEIVER (Cont'd)

Error Detector Parameters	
Pulses:	Flashes at a maximum rate of 10 per second to indicate the presence of pulses.
Bipolar Violations:	Flashes up to a maximum rate of 10 per second to indicate violations in T1 and T1C systems. In T148 systems, indicates disparity errors.
Logical Errors:	Flashes once for each logical error found in bit-by-bit examination of QRSS signal; up to maximum of 10 per second.
Oscillations:	Flashes to indicate presence of 1 to 20 kHz (nominal 10 kHz) oscillations (squarewave), or "all ones" oscillations.
Input Impedance:	200 ohms.
Input Dynamic Range:	0.3 to 3.3 V peak.
Error Detector Output Jack:	TTL compatible.

REPEATER TEST PARAMETERS

Powering Current:	Adjustable from 50 to 220 mAdc.
Meter Indications	
Current:	0 to 220 mAdc.
Repeater Voltage Drop:	0 to 22 Vdc.
Meter Accuracy:	± 5% of full scale.
Artificial Line:	Provides selectable attenuation steps of 5, 9, 16, 24, 31, 33, 36, 38, 40, and 43 dB at 772 kHz.
Interference (NEXT):	Sinewave level adjustable in 1-dB steps from 8 to 18 dB (± 0.5 dB) below level of all ones signal at repeater input. T1 freq = 770 kHz, T1C freq = 1570 kHz, T148 freq = 1182 kHz. Tolerance = +0, −5%.
High Voltage Leakage Test:	Applies 200 Vdc ± 20%; indicator lights when insulation resistance is less than 1 megohm ± 50%.

GENERAL

Environmental	
Operating Temperature Range:	0°C to +50°C (32°F to +122°F).
Storage Temperature Range:	−40°C to +75°C (−40°F to +167°F).

Table 2—1. (Cont'd)

GENERAL (Cont'd)

Environmental (Cont'd)	
Relative Humidity:	0 to 95%, noncondensing.
Power Requirements:	115 Vac ± 10%, 60 Hz, ± 10%; approx. 30 watts.
Size:	13 in. w x 9 in. h x 11 in. d (33 cm. x 22.9 cm. x 27.9 cm).
Weight:	Approximately 20 pounds (9.1 kg).

SECTION 3

CONTROLS, INDICATORS, AND JACKS

3.1 This section contains a description of the controls, indicators, and jacks shown on Figure 3—1 and listed in Table 3—1.

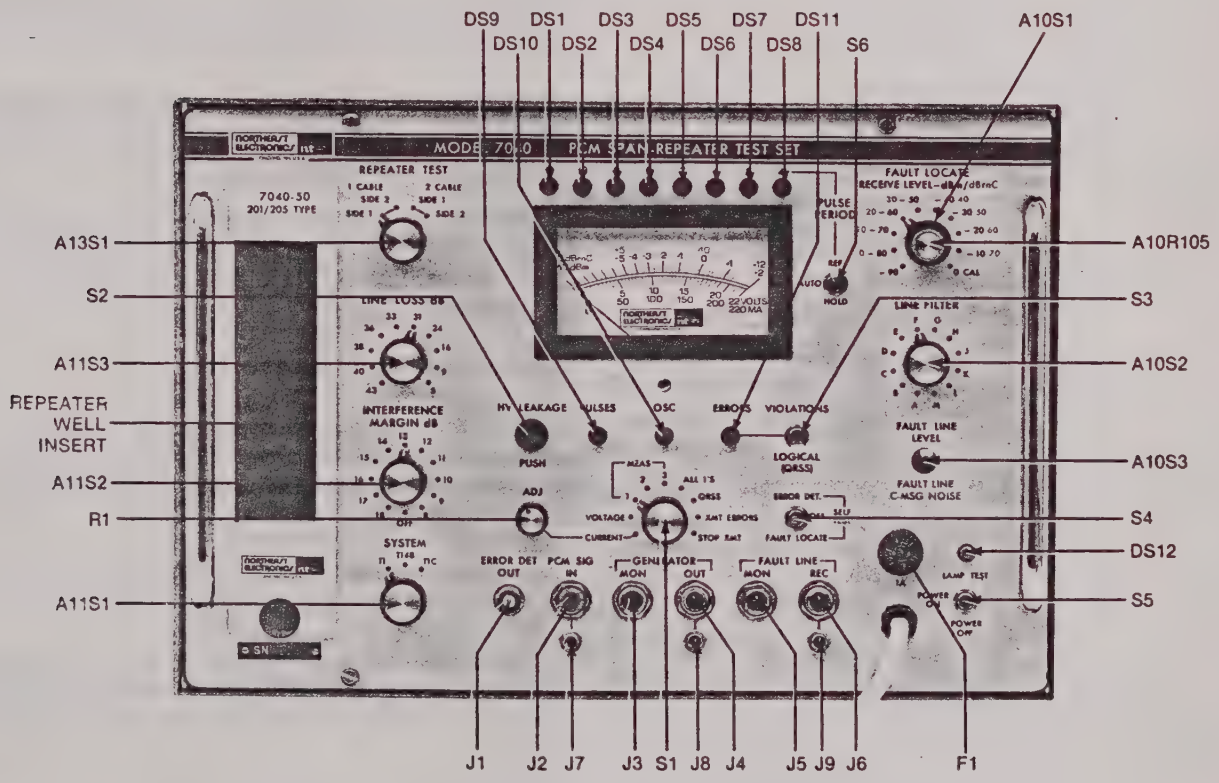

Figure 3—1. Model 7040 Controls, Indicators, And Jacks.

Table 3—1. Model 7040 Controls, Indicators And Jacks

REFERENCE DESIGNATION	CONTROL, INDICATOR OR JACK	FUNCTION
DS1-DS8	PULSE PERIOD indicators	When any one is lighted, it indicates the pulse density of a MEAS 1, 2, or 3 pattern being generated by the 7040. For example, when the 11 indicator (DS1) is lighted, the 7040 is producing a pattern with one pulse trio per 11 time slots.
DS9	PULSES indicator	When flashing, indicates presence of pulses at J2 or J7 or at the output of a repeater in the test well.
DS10	OSC indicator	When flashing, indicates presence of nominal 10-kHz or "all ones" oscillation at J2 or J7 or at the output of a repeater in the test well.
DS11	ERRORS indicator	When flashing, indicates presence of either bipolar violation (T1/T1C) or disparity (T148) errors or QRSS logical errors at J2 or J7 or at the output of a repeater in the test well.
DS12	Power indicator	When lighted, indicates that the 7040 is turned on.
J1	ERROR DET OUT jack	A BNC connector for use in monitoring, recording, or counting all detected errors . . . either bipolar or logical. A TTL-compatible logic-low pulse appears at J1 for each detected error.
J2 & J7	PCM SIG IN jacks	Type 310 and bantam jacks for use in monitoring a PCM span line for pulses, errors, and oscillations.
J3	GENERATOR MON jack	A 310 jack for use in monitoring the 7040 PCM signal generator output. Tip and ring each have 430-ohm resistors in series for compatibility with office error detector.
J4 & J8	GENERATOR OUT jacks	Type 310 and bantam jacks for connecting the 7040 PCM generator output to a span line under test. The test signal pattern is controlled by S1.
J5	FAULT LOCATE MON jack	A 310 jack for use in monitoring the audio signal(s) present on a fault locating pair. Can be used with a high impedance headset or similar monitoring device.
J6 & J9	FAULT LINE REC jacks	Type 310 and bantam jacks for connecting the 7040 to a fault locating pair.
M1	Meter	Indicates repeater powering current (mA), or repeater voltage drop (V), or audio fault locating tone level (dBm), or C-message noise (dBrnC) . . . depending on setting of switch S1 and type of test.
R1	CURRENT ADJ control	Sets operating current appropriately for a repeater in the test well. When S1 is at CURRENT position, the repeater operating current is indicated on meter M1.

Table 3—1. (Cont'd)

REFERENCE DESIGNATION	CONTROL, INDICATOR OR JACK	FUNCTION
S1	Function switch	Selects the function to be performed by the 7040 as follows: 1. CURRENT position selects measurement of powering current supplied to a repeater in the test well; current is shown on meter M1 and is adjustable via R1. 2. VOLTAGE position selects measurement of powering voltage drop across a repeater in the test well. 3. MEAS 1, 2, and 3 positions select corresponding MEASURE pulse patterns for application to a span line or individual repeater under test. Audio modulating frequency for the MEASURE patterns is selected by LINE FILTER switch A10S2. 4. ALL 1's position selects an all ones test signal pulse pattern for application to a span line or individual repeater under test. 5. QRSS position selects a quasi-random test signal pulse pattern for application to a span line or individual repeater under test. 6. XMT ERRORS position selects a QRSS pulse pattern into which deliberate errors are introduced about every ⅔ second. This corresponds to a bit error rate of 10^6 at a 1.544 Mb/s clock rate. 7. STOP XMT position stops the 7040 generator output signal.
S2	HV LEAKAGE pushbutton/lamp	When pressed and held, applies 200 Vdc between case and powering circuit ground of a repeater in the test well. This checks the insulation resistance. A lamp in the HV LEAKAGE pushbutton will light if insulation resistance is less than 1 megohm ± 50%.
S3	VIOLATIONS/LOGICAL (QRSS) switch	1. VIOLATIONS position causes any detected bipolar violation errors (T1/T1C) or disparity errors (T148) to appear as flashes of ERRORS indicator DS11. 2. LOGICAL (QRSS) position causes any logical errors detected in bit-by-bit checking of a T1 QRSS pattern to appear as flashes of ERRORS indicator DS11.
S4	SELF TEST switch	1. OFF is normal position for regular use of the 7040; the self test feature is disabled. 2. ERROR DET position is used for self checking the 7040 error detection functions. 3. FAULT LOCATE position is used for self checking the 7040 circuits which monitor/measure the audio tones on a fault locating pair.

Table 3—1. (Cont'd)

REFERENCE DESIGNATION	CONTROL, INDICATOR OR JACK	FUNCTION
S5	POWER/LAMP TEST switch	1. POWER OFF position removes ac input power from the 7040. 2. POWER ON position applies ac input power to the 7040. LED indicator DS12 should light. 3. LAMP TEST position checks front panel indicators DS1 through DS11. All these indicators should light.
S6	PULSE PERIOD REF/ AUTO/HOLD switch	Selects the stepping mode for pulse density variation when using MEAS 1, 2, or 3 test signal pulse patterns. 1. REF position fixes pulse period at 11. 2. AUTO position starts pulse period at 11, then automatically steps pulse period to 4. 3. HOLD position continuously holds pulse period at the number (11 through 4) which was present when the HOLD position was selected.
A10R105	Variable sensitivity control	When fully clockwise at CAL position, meter M1 shows absolute level (dBm) or noise (dBrnC) within the range selected by A10S1. Variable control can also be used to set meter at a reference level, such as 0, for comparative measurements.
A10S1	FAULT LOCATE RECEIVE LEVEL dBm/dBrnC switch	The blue outer dBrnC scale sets sensitivity of the 7040 noise measuring receiver. The black inner dBm scale sets sensitivity of the 7040 level measuring receiver used for fault locating.
A10S2	LINE FILTER	Selects the fault locating filter code (frequency) to be used. This adds correct audio tone component to the 7040 generator's MEAS 1, 2, or 3 output, and also conditions the 7040 receiver to "tune-in" only the selected audio frequency.
A10S3	FAULT LINE LEVEL/ FAULT LINE C-MSG NOISE switch	Selects either the level or noise measuring circuits of the 7040 to check a fault locating pair at J6/J9 . . . or a repeater in the test well.
A11S1	SYSTEM switch	Conditions the 7040 for testing at a T1 (1.544 Mb/s), T148 (2.37 Mb/s), or T1C (3.152 Mb/s) bit rate.
A11S2	INTERFERENCE MARGIN dB switch	Selects an interfering signal amplitude (in dB below a nominal all 1's signal level) that is superimposed on the test signal applied to a repeater in the test well. This allows checking of repeater performance with Near-End-Cross-Talk (NEXT) at the repeater input. The interfering signal is removed when the switch is at OFF position.

Table 3—1. (Cont'd)

REFERENCE DESIGNATION	CONTROL, INDICATOR OR JACK	FUNCTION
A11S3	LINE LOSS dB switch	Selects the amount of artificial line loss (in dB) to be placed in series with a repeater in the test well. This simulates cable loss so that repeaters can be tested under realistic operating conditions.
A13S1	REPEATER TEST switch	Selects the correct electrical interface wiring to accommodate either 1 CABLE (bidirectional) or 2 CABLE (unidirectional) repeaters in the test well. Also selects either SIDE 1 or SIDE 2 of a line repeater for testing.

SECTION 4

THEORY OF OPERATION

4.1 This section contains the theory of operation for the Model 7040 PCM Span-Repeater Test Set. Three levels of description are provided. They are (1) an overall block diagram description, (2) a series of functional section descriptions, and (3) a series of detailed circuit descriptions.

4.2 OVERALL FUNCTIONAL DESCRIPTION

4.3 As shown on Figure 4—1 the Model 7040 is comprised of three functional groups. These are: (1) the transmit functions, (2) the receive functions, and (3) the repeater test functions. These are shown as the large shaded areas on the illustration. Interconnection of the functional sections is via the GENERATOR OUT, PCM SIG IN, and the FAULT LINE REC jacking arrangement.

4.4 TRANSMIT FUNCTIONS

4.5 The transmit functional group generates the test signals used to test external PCM equipment, to test repeaters plugged into the adapter well, and to check the receive functions during self test.

4.6 As directed by the function and SYSTEM switches, the control logic generates signals that are used to set the bit rate and the signal format produced by: (1) the QRSS and ALL 1's signal generator, and (2) by the MEAS 1, 2, 3 fault locate signal generator. Bit rates for the three common PCM systems of T1, T1C, and T148 are selected by the SYSTEM switch. The signal formats available (as selected by the function switch) are the MEAS 1, 2, 3 signals for use in span line fault locating as well as repeater pre-installation testing; the ALL 1's signal which is useful to keep repeaters from oscillating; and the general-purpose QRSS signal. Also available are the QRSS signal containing deliberate errors and a stop transmit function, both of which are useful in identifying particular span lines. An output of the control logic is also used to set the bit rate of the ALL 1's signal generator in the repeater test function.

4.7 The LINE FILTER switch determines the frequency of the audio component impressed onto the fault locate signal generator output. The 12 standard letter-coded filters A-M, providing audio components within the range of 832 Hz to 3017 Hz, are available. An additional output of the fault locate signal generator is the fault locate receiver tuning signal. This insures that receiver tuning is always exactly correct for the fault locate audio signal being transmitted. Cycling of the pulse period (11 through 4) is under control of the PULSE PERIOD switch. The pulse period being used at any instant is displayed by the PULSE PERIOD indicators.

4.8 Either the output of the QRSS and ALL 1's signal generator or the output of the fault locate signal generator is applied to GENERATOR OUT jacks J4 and J8. These 310-type and bantam-type jacks provide the access normally used to test external PCM equipment. MON jack J3 is normally used to connect an office error detector to check the signal generator output. Note that a plug inserted into either GENERATOR OUT jack breaks the signal path from the transmit function to the repeater test function. The MON jack, however, is always connected to the signal generator output so that it can be used at any time. The self test signal is always connected to the receive function and is discussed in the following paragraphs.

4.9 RECEIVE FUNCTIONS

4.10 The receive function consists of an error detector and a fault locate receiver. Each of these is discussed separately.

4.11 The input to the error detector is normally the PCM signal being supplied by whatever PCM equipment is being tested. Either a type-310 or a bantam-type access jack, labeled PCM SIG IN can be used for this purpose. Note that a plug in either jack breaks the path from the repeater test function which can also supply the input. The so-called error detector is actually three detectors: (1) a pulse detector, (2) an all ones and 10 kHz oscillation detector, and (3) a logical (QRSS) and bipolar violations/disparity error detector. The presence of a normal PCM signal input causes the PULSES indicator only to be lighted. A PCM signal that has either bipolar violations or disparity errors (T148) in its bit stream will light both the PULSES and ERRORS indicators when the VIOLATIONS/LOGICAL (QRSS) switch is in the VIOLATIONS position. If this switch is set to LOGICAL (QRSS), and there are logical errors in the bit stream, then both the PULSES and ERRORS indicators will be lighted.

NOTE

It should also be noted that since the MEAS 1, 2, and 3 signal formats have deliberate bipolar violations present, the ERRORS indicator will flash whenever these signals are used. This is normal.

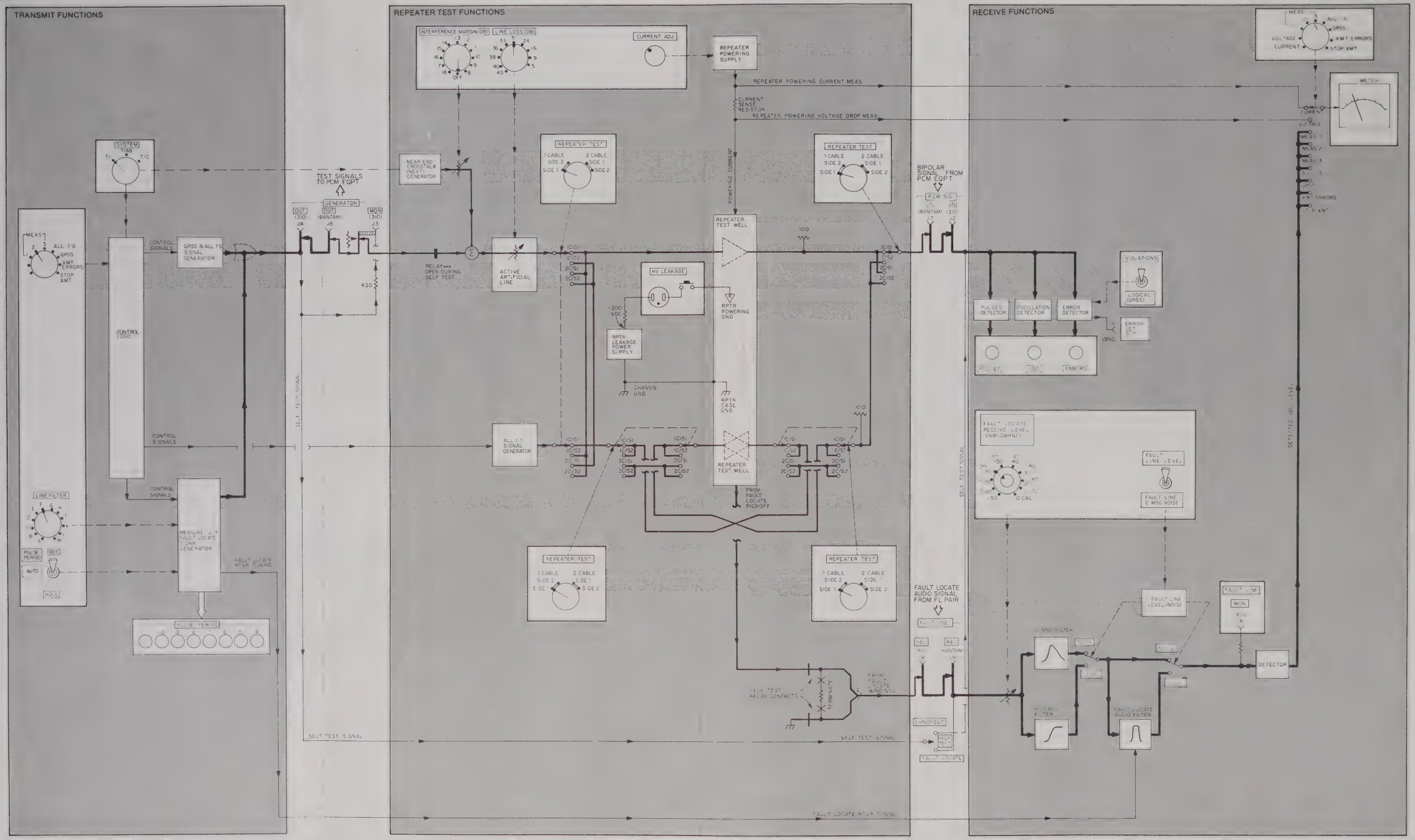

Figure 4—1. Model 7040 Functional Block Diagram

4.12 If 10 kHz oscillations are present, only the OSC indicator will be lighted. If both the OSC and the PULSES indicators are lighted, the presence of all ones oscillations is indicated. ERROR DET OUT BNC connector J1 allows a recording/counting device to be connected to the error detector output.

4.13 The audio or noise taken from a fault locate pair can be applied to the fault locate receiver through either a 310-type or a bantam-type jack labeled FAULT LINE REC. Note that a plug inserted into either of these jacks breaks the fault locate signal path from the repeater test functions, which can also supply the input. The FAULT LOCATE RECEIVE LEVEL (dbm/dbrnc) range switch inserts the appropriate amount of attenuation into the signal path ahead of the filters. Available noise ranges are 0 to 70 dBrnC; level ranges are −90 to 0 dBm. When the FAULT LINE LEVEL/FAULT LINE C-MSG NOISE switch is in the FAULT LINE C-MSG NOISE position, the noise response is shaped by the C-message filter before being applied to the detector. For all positions of the function switch except CURRENT and VOLTAGE, the detector output is displayed on the meter.

4.14 To measure the fault locate signal level, the FAULT LINE LEVEL/FAULT LINE C-MSG NOISE switch is set to FAULT LINE LEVEL. The audio component of the fault locate signal is first applied to a highpass filter to remove any induced low-frequency power line hum. It is next applied to an audio filter that is tuned to the desired frequency by the fault locate receive tuning signal furnished by the transmit function. The filter has an extremely narrow bandpass and only the audio frequency that was transmitted is passed on to the detector. The detector output is then displayed on the meter. A 310-type FAULT LINE MON jack is provided to monitor the fault line pair with a high-impedance device such as a headset or an oscilloscope.

4.15 A self test feature has been incorporated into the receive function. A self test signal furnished by the transmit function is applied to the SELF TEST switch. When the switch is set at ERROR DET, the error detector is exercised and the indicators are lighted depending on the signal format selected. In the FAULT LOCATE position, all of the circuits in the fault locate receiver (except the C-message filter) are checked.

4.16 REPEATER TEST FUNCTIONS

4.17 As shown on Figure 4−1, the repeater test function is situated between the transmit and receive functions and uses the series-connected access jacks for interconnection. Since the repeater tests rely on both of these functions, all jacks must be empty to perform repeater tests.

4.18 The repeater under test is inserted into the repeater test well, which is designed to accept many types of repeaters through the use of adapters. After inserting the repeater under test into the adapter, the correct operating current must first be set. This is done by setting the function switch to the CURRENT position and then setting the CURRENT ADJ potentiometer to obtain the correct indication on the meter. Next the function switch is set to VOLTAGE to observe the voltage drop across the repeater. To check the leakage to repeater powering ground, −200 Vdc is connected through a resistor, a neon lamp, and a pushbutton switch to ground. When the pushbutton is closed, the neon lamp will light only if the insulation resistance (leakage) is below a specified limit.

4.19 Both 1-cable (bidirectional) and 2-cable (unidirectional) repeaters can be accommmodated in the test arrangement. The five sections of the REPEATER TEST switch shown on Figure 4−1 route the signals into and out of the repeater in the correct directions when testing sides 1 or 2. The side being tested is supplied any of the available signal formats from the transmitter function through an active artificial line. Under control of the LINE LOSS (dB) switch, the artificial line can simulate line losses within the range of 43 to 5 dB at T1 line bit rates. Whichever side of the repeater is not being tested is supplied an all ones signal to keep its regenerator from oscillating.

4.20 The side of the repeater being tested is properly terminated in 100 ohms and the signal is then applied to the error detector section of the receive function for pulses, errors, and oscillation checks. The fault locate pickoff winding is brought out and applied through a normally-closed set of relay contacts before being sent to the fault locate receiver section of the receive function for the merit test. During self test, a resistor is placed across the input of the fault locate receiver through normally-open relay contacts. This provides the correct termination for the self test signal source located in the transmitter function.

4.21 When measuring Near-End Crosstalk (NEXT), the output of the NEXT generator is summed with the signal from the transmitter function before being applied to the artificial line and then to the repeater under test. The INTERFERENCE MARGIN (dB) switch provides levels within the range of 18 to 8 dB below an all ones signal.

4.22 TRANSMIT SECTION FUNCTIONAL DESCRIPTION

4.23 See Figure 6−1 for the functional schematic diagram of the transmit section. The function of the transmit section is to generate all of the signal formats

used to test external equipment, repeaters inserted in the test well, and for self test. Sub functions included in the transmit function are the transmit clocks, the QRSS generator, the T148 generator, the fault locate generator, and the repeater idle side QRSS generator. The switching control functions are distributed among all of the sub functions.

4.24 TRANSMIT CLOCKS

4.25 The function of the transmit clock circuit is to generate and select the basic frequencies that are used by the QRSS generators, the T148 generator, and the digital fault locate generator. Selection of the basic frequency is done by SYSTEM switch A11S1. For example, when T1 is selected, the input of U4C located on A5 is grounded and the inputs of U7A and U7B are pulled up to +5 Vdc. This enables U4C and inhibits U4A and U4D. As a result, only the output of 6.176 MHz oscillator Q1/Q4 is applied through U1A to counter U6A/B. The output of the counter is called CLOCK(X) and is at the exact bit rate for T1 and T1C when selected. This is then applied to the fault locate generator, the repeater idle side QRSS generator, and to the multiplexer located on A4.

4.26 When selecting T148, the 4Xϕ output of U1A is at four times the final T148 bit rate, or 9.48 MHz. This is applied to the T148 generator located on A6.

4.27 When either T1 or T1C is selected, the H input of U1A located on A4 is low. This forces the U1A output high, which in turn, forces the output of U2F low. This selects the A input function of multiplexer U4. Thus the CLOCK(X) signal is selected and present at the 3Y output that is then applied to the QRSS generator located on A2.

4.28 When T148 is selected by A11S1 and either QRSS or XMT ERRORS is selected by function switch A12S1, both inputs of U1A located on A4 are high. This forces its output low, which is inverted by U2F, and enables the select B function of multiplexer U4. This selects the T148 transmit clock generated on A6 and makes it available at the 3Y output of the multiplexer. It is then used by the QRSS generator located on A2.

4.29 QRSS TRANSMIT GROUP

4.30 The function of the QRSS transmit group is to generate the signals associated with T1 and T1C for the QRSS, all ones, and error modes of operation. It also generates a basic QRSS signal used to generate the T148 QRSS signal.

4.31 The heart of the function is the QRSS pattern generator. This circuit uses the XMT CLOCK input to generate the Bell System standard quasi-random word format that is 1,048,575 bits long. The word length and the quasi-random nature of the bit stream are a result of returning bits 17 and 20 to the serial input of the shift register through an exclusive OR gate. Fifteen zero suppression is provided by the 15 zero detector for both T1 and T148. When this condition occurs, logical ones are stuffed into the bit stream through U14D. Suppression is inhibited by the T1C SEL input for the T1C function. A 20 zero detector prevents a potential lockup mode at turn on.

4.32 Decoding of the $\overline{\text{QRSS}}$ and $\overline{\text{XMT ERRORS}}$ inputs by U2C enables U2B so that the QRSS OUT signal from the pattern generator is applied to the double rail-to-single rail converter and the T148 generator. This signal is present for T1, T1C, and T148. Additional decoding of the $\overline{\text{111}}$, $\overline{\text{T148 SEL}}$, and the $\overline{\text{MEAS}}$ inputs by U2D and U2A causes the single rail-to-double rail converter to output the T1 and T1C QRSS signal when requested. When the all ones output is called for, the output of U2A inhibits the QRSS signal and forces the output of the converter to be all ones. This applies to T1, T1C, and T148. The converter output is gated through U16A/B.

4.33 When A12S1 is set to XMT ERRORS, U1A enables U1C located on A5. The output of 1.5-Hz oscillator U7C/U10 is now applied to the error inserter circuit located on A2. This results in the deletion of one pulse from the T1 and T1C QRSS signal approximately every 1.5 seconds. In circuits farther down stream, this results in one bipolar violation for each pulse deleted.

4.34 T148 GENERATOR GROUP

4.35 The function of this group is to convert the basic T148 QRSS signal furnished by A2 to the unique T148 format and to insert errors into the bit stream when requested to do so. The basic input to the group is the 4Xϕ (9.48 MHz) signal supplied by A5. This is used to generate the T148 XMT CLOCK and the timing signals designated A through D. The timing signals are used throughout the T148 generator group to accomplish the complex timing functions required. The T148 XMT CLOCK is used by the T148 generator circuits and is also sent to the clock multiplexer located on A4. This clock is the basic T148 clock signal from which the QRSS generator makes the basic T148 QRSS signal.

4.36 The T148 XMT DATA input from A2 is a continuous bit stream in the standard QRSS format. The function of the T148 generator is to convert 4-bit groups of this signal to specially-coded 3-bit ternary groups. This is accomplished by shifting four bits into shift register U5 and momentarily halting the operation to make the ternary conversion.

The four bits stored in the shift register, along with a fifth bit supplied by the disparity controller/error generator, are used to address a particular location in ROM (Read Only Memory) U10. Stored in this location are two, 3-bit parallel words designated D1, D2, and D3 and D4, D5, and D6. Each word is latched into its associated shift register; either U18 or U19. Using the $\overline{B}$ timing signal, the bits are then shifted out one at a time. The two, 3-bit groups are then applied to a disparity controller/error generator, which controls the encoding scheme that is peculiar to the ternary format. Thus a closed-loop system is formed that makes the encoding of the next group dependent on the past history of all previous groups.

4.37 When T148 is selected by A11S1 and when either QRSS or XMT ERRORS is selected by A12S1, the output of U1A located on A4 goes low. This is applied to the enable input of T148 output gates located on A6. The T148 tip and ring bit streams are passed by the gates and applied to the output gates located on A2.

4.38 Both logical and disparity errors are forced into the T148 bit stream in the following manner. When A12S1 is set to XMT ERRORS, the error oscillator located on A5 generates an error pulse approximately every two thirds of a second. This is applied to both the logical and the disparity error generators. Logical errors are generated by eliminating a logical one from the T148 QRSS bit stream applied to 4-bit shift register U5. The #19 input to the logical error generator is one bit time ahead of the QRSS input. This is used to condition the logical error generator so that it will eliminate the next logical one that appears in the QRSS bit stream. This is the definition of a logical error; i.e. either eliminating or creating a bit where one either did or did not exist.

4.39 Normally the 3-bit words selected by ROM U10 are partially controlled by the disparity controller through the use of a line applied to the most significant bit input (A) of U10. When an error is requested, the disparity error generator causes the disparity controller to alter its output in such a manner that the next 3-bit words selected by the ROM force a single disparity error. This error is alternated from positive to negative.

4.40 FAULT LOCATE GENERATOR

4.41 The main function of the fault locate generator, located on A8, is to provide the fault locating signals in their various forms. The four parameters that can be altered are the bit rate, audio frequency component, the format, and the pulse density.

4.42 The basic bit rate is supplied as CLOCK (X) generated on A5. This is inverted by U7C to form $\overline{\text{CLOCK (X)}}$, which is the basic clock for the measure 1, 2, and 3 waveform pattern generator and the pulse period zero counter functions.

4.43 The audio frequency component is synthesized by programming a preset counter and then counting the basic 1.544 MHz clock signal. The division ratios for the fault locate audio generator are selected by LINE FILTER switch A10S2. The generator furnishes four outputs designated FLDS1, FLA, FLB, and FLC. All four are applied directly to the fault locate receiver. In addition, FLC is the basic audio frequency that is used to modulate the basic bit stream. This signal is applied directly to the measure 1, 2, and 3 waveform pattern generator.

4.44 The third parameter that can be controlled is the pulse period (density). Pulse densities of one triad per eleven time slots to one triad per four time slots are available. This function is controlled by the setting of PULSE PERIOD switch A12S6. The technique used to generate the pulse density is to generate a single pulse triad and then insert from one to eight logical zeros.

4.45 When A12S6 is set to REF, the pulse period step counter is reset to zero, which also presets the pulse period zero counter to zero. The triad generator now generates one triad that occupies three time slots. The pulse period counter counts to eight, during which time eight logical zeros are generated. This is the definition of pulse period 11; one triad followed by eight logical zeros.

4.46 When A12S6 is set to AUTO, the pulse period step counter totalizes the pulses generated by the stepping oscillator. The pulse rate is approximately one pulse per five seconds. Each time the output of the step counter changes, the zero counter is preset to a number that is one higher than the preceding number. Since the zero counter always overflows at the count of eight, the number of digital zeros inserted between triads is progressively decreased from eight to one. At pulse period four, the cycle halts until the PULSE PERIOD switch is again set to REF and then to AUTO. Any time during auto cycling that A12S6 is set to HOLD, the step counter halts at its present count and the pulse period corresponding to this count is generated continuously.

4.47 To identify the pulse period presently being sent, a series of indicator lamps is used. The three-line, BCD output of the step counter represents the current pulse period being generated. This information is decoded in a BCD to decimal decoder, which then lights the appropriate indicator lamp. A lamp test mode is provided where a lamp test signal causes all of the pulse period indicator lamps to light. The BCD output of the step counter is also made available to the fault locate receiver to alter its gain versus pulse period.

4.48 The fourth and last parameter of the fault locate signal that can be varied is the format; i.e. either measure 1, 2, or 3. The input from A12S1 is decoded and causes the measure 1, 2, and 3 generator to generate either positive triads or negative triads, which are then assembled in the correct order. The tip and ring fault locate signals are then applied to the output gate located on A2.

4.49 REPEATER IDLE SIDE GENERATOR

4.50 To prevent oscillations in the idle side of a repeater under test, an all ones signal is applied to this side of the repeater. The all ones generator is located on A2. The signal is attenuated and then transformer-coupled to the repeater test circuits located on A13.

4.51 PCM RECEIVE SECTION FUNCTIONAL DESCRIPTION

4.52 See Figure 6–2 for the functional schematic diagram of the PCM receive section. The function of the PCM receive section is to detect bipolar violations, oscillations, logical errors, and disparity errors. The results are displayed using front panel indicator lamps.

4.53 PULSE RECOVERY

4.54 The function of the pulse recovery circuits is to generate two unipolar pulse streams from the bipolar PCM input. During normal operation, the input is taken from the PCM line under test through either PCM SIG IN jack J2 or J7. The signal can also come from a repeater under test if a plug is not inserted in either J2 or J7. The input signal is converted into two bipolar bit streams referenced to ground by pulse transformer T1A located on repeater test board A13. High-voltage transients on the input are protected against by protective devices CR12 through CR16. Variable threshold detector U3 and U6 generates a voltage that is always exactly one half of the long-term average of the peak level. This is applied as a reference voltage to voltage comparators U4 and U5. When the pulse input to either comparator is more positve than the reference, the comparator output goes low. Inverters U2A/B provide a stream of positive unipolar pulses that represent both the positive and the negative pulses as they existed on the input. These outputs are labled +PULSES and −PULSES respectively. The two pulse streams are combined by U2C to form $\overline{\text{DATA}}$, while DATA is formed by inverter U2D.

4.55 CLOCKS

4.56 The function of the clock circuit is to generate T1, T1C, and T148 clock pulses that are used in these functions, clock recovery from the received pulse stream, and T1 and T148 data recovery.

4.57 SYSTEM switch S1, located on Artline assembly A11, applies ground to one of the three clock generators located on A5. Only the grounded clock generator provides an output that is applied to U1A. The output of this gate is designated 4Xϕ and is used throughout the receive circuits.

4.58 Recovering clock pulses that are synchronous with the received data is the function of the clock recovery circuit comprised of U2, U5, and U8. Inputs to the clock recovery circuit are DATA, $\overline{\text{DATA}}$, and 4Xϕ.

4.59 The T148 pulse recovery circuit is comprised of U3A through U3D. Inputs are the +PULSES, −PULSES, and the recovered clock. The outputs are a pair of unipolar pulse trains designated T148 +PULSES and T148 −PULSES. These are used by the T148 data recovery and disparity error circuits.

4.60 DATA and 4Xϕ inputs are applied to T1 data recovery circuit U2A and U5A/B. This output is designated T1 DATA.

4.61 T148 RECEIVER

4.62 The function of the T148 receiver, located on A7, is to recover the T148 data and the associated clock and to detect disparity errors. Both of these circuits have as inputs the T148 ±PULSES, CLOCK(R), and 4Xϕ. The T148 data recovery circuit consists of portions of U2-U4, U7, and U9-U14. The T148 REC CLOCK and T148 REC DATA outputs are used by the logical error detector. The T148 disparity error detector is comprised of portions of U1, U2, U5, U6, and U8. The output is designated DISPARITY ERRORS and can be selected for display by the ERRORS indicator.

4.63 INTERFACE

4.64 The function of interface assembly A4 is to detect bipolar violations and oscillations and to interface with the ERRORS, PULSES, and OSC indicators located on the front panel.

4.65 Bipolar violation detector U3A, U7A/B, and U7D analyzes the ±PULSES and the DATA inputs and generates a pulse whenever a violation is detected. This output is applied to multiplexer U4, which selects either bipolar errors or disparity errors.

4.66 Both oscillation detectors scan the −PULSES input for either low frequency (less than approximately 20 kHz) or all ones oscillations. The 20 kHz oscillation detector consists of U2A and U6C/D. Outputs from these detectors are then applied to select gates.

4.67 Error select gate U2E and U8, oscillation select gate U1C, U5A, and U9C, in conjunction with multiplexer U4 determine which of the front panel indicators will be lighted. When SYSTEM switch S1 is set to T148,

U1A and U2F cause multiplexer U4 to select the DISPARITY ERRORS input and apply it to the error select gate. For the other positions of S1, U4 selects the bipolar violations line. When oscillations of 20 kHz or lower are detected, the output of the 20 kHz oscillation detector inhibits the error select gate since the errors that will be detected are meaningless for this condition. Each pulse at the output of the error select gate triggers LED error duty cycle generator U12, which sets the LED on time to approximately 50 percent. The ERRORS indicator is driven through decode gate U9B, which allows the indicator to be turned on when the POWER switch is set to the LAMP TEST position. The output of the error select gate is also applied to counter buffer U5B and made available at the ERROR DET OUT jack for external monitoring purposes.

4.68 Oscillation select gate U1C, U5A, and U9C provides an output when there is either 20 kHz or less oscillations or when there is all ones oscillation during the time that SYSTEM switch S1 is in the T1 position. This output enables oscillation LED decode gate U1C, U5D, U7C, U9C/D, and U15A. Another input to the decode gate is the output of oscillation and pulses LED duty cycle generator U11, which is triggered by the DATA pulse stream. Thus the OSC indicator will have an on time of approximately 50 percent during oscillation conditions. The decode gate also allows the indicator to be tested.

4.69 The output of U11 is also applied through pulses LED decode gate U9A, which drives the PULSES indicator. Again, the decode gate allows the indicator to be tested.

4.70 QRSS RECEIVER

4.71 The function of the QRSS receiver is to compare, bit-by-bit, the received QRSS data with an internally-generated QRSS pulse stream and generate a bit error each time the two do not agree. These are called logical, or bit errors. Provision is made for initial synchronization of the two QRSS signals.

4.72 Assuming that the two QRSS signals have been synchronized and that there are no logical errors occurring, bit 20 at the output of the 20-bit delay circuit will be in agreement with bit 20 at the output of the QRSS generator. Thus there will be no bit errors at the output of the logical error detector. Each time there is a bit disagreement, a bit error is generated. This is applied to the interface board where it is processed for display and also to the error rate detector. As long as the error rate remains below approximately one percent, any bit errors are assumed to be the result of legitimate logical errors in the received data. When the bit error rate exceeds this level, it is assumed that the two QRSS signals are out of synchronization. The internal feedback is removed from the QRSS generator input and in its place is substituted the received data. Since the 20-bit delay and the QRSS generator are both now functioning as 20-bit shift registers, they will be in exact agreement if at least 20 bits of the received data are shifted in. At this time the sync switch again allows the internal feedback to drive the QRSS generator and the two QRSS signals are synchronized at this instant. Normal operation with bit error detection now proceeds.

4.73 ANALOG FAULT LOCATE RECEIVER FUNCTIONAL DESCRIPTION

4.74 See Figure 6–3 for the functional schematic diagram of the analog fault locate receiver. The function of the analog fault locate receiver is to select one of 12 audio fault locate signals and convert it to a proportional dc-voltage suitable for display on a meter.

4.75 When fault locating on a PCM span line, the returned fault locate signal from the line would be applied through either FAULT LINE REC jack J6 or J9. During repeater testing, the fault locate signal from the repeater is applied through J6 and J9 as long as there is no plug in either of these jacks. When SELF TEST switch S5 is set to FAULT LOCATE, a PCM signal containing a fault locate audio component is applied to the receiver.

4.76 The balanced fault locate signal is first applied to T2, which converts the input to a single-ended signal referenced to ground. During a self test, T2 effectively removes most of the high frequency carrier component of the PCM signal and passes only the audio fault locate component. The other two sources are audio when they enter the unit. The first step in normalizing the −90 dBm to 0 dBm dynamic range of the input signal is performed by the 40-dB attenuator and switch S1A. This is followed by +10 dB amplifier U1.

4.77 Normally the noise on the fault line is measured prior to proceeding with the actual fault locating procedure. When FAULT LINE switch S3 is set to C-MSG NOISE, relay K2 energizes and applies the output of U1 through the C-message filter to RECEIVE LEVEL adjustment R105. When S3 is set to LEVEL during fault locating, K2 is not energized and the output of U1 is applied through the 60 Hz reject filter.

4.78 To obtain absolute meter readings in dBm or dBrnc, RECEIVE LEVEL adjustment R105 is set fully clockwise to the CAL position. The second step in normalizing the input signal dynamic range is provided by the fine attenuator and S1B after first being amplified 20 dB in amplifier U2. The 90 dB dynamic range of the input signal has now been compressed to a 10 dB range for every position of S1.

4.79 As the digital fault locating signal is cycled from pulse positions 11 through 4, the amplitude of the analog audio component returned increases. This is due to the increased pulse density at the lower pulse position numbers. To counter this increase that might mask true variations caused by faults, the gain of pulse period gain control stage U3 is made to vary as the pulse period changes. Digital fault locate board A8 provides pulse period switching information encoded in BCD and designated as PPA, PPB, and PPC. Depending on the actual pulse period selected at any given instant, the analog switch selects the appropriate combination of resistors that are part of the feedback network determining the gain of U3. The gain varies from approximately +35 dB at pulse period 11 to +25.5 dB at pulse period 4. The output of U3 is further amplified by 20 dB in U4A and U4B and transformer coupled by T1 for application to either the bandpass filter or the detector.

4.80 When FAULT LINE switch S3 is set to LEVEL, the output of T1 cannot pass through the normally-closed contacts of K1, which is not energized. In this case, the fault locating audio must pass through the filtering components before being converted to a dc voltage. When S3 is set to C-MSG NOISE, K1 is energized and the noise signal is applied directly to the detector.

4.81 Since the audio fault locating signal is at a very low level, the signal-to-noise ratio can be improved greatly by use of a narrow bandwidth. This is accomplished with an audio, digital, commutative bandpass filter that has a bandpass of 1 ± 1 Hz. The center frequency of the filter is digitally selected by the four-line BCD information supplied by A8. After being buffered by voltage follower U10A, additional filtering is provided by selectable active low-pass filters. The appropriate filter that matches the line filter letter being used is selected by LINE FILTER switch S2.

4.82 The detector converts the audio fault locate signal to a proportional dc voltage. The signal is displayed on meter M1 located in the feedback path of meter driver U7B. MEAS 1, 2, and 3 are the positions used during fault locating. The fault locate audio signal is also applied to FAULT LINE MON jack J5. This allows the signal to be monitored by external devices such as an oscilloscope, a meter, or a recorder.

4.83 REPEATER TEST SECTION FUNCTIONAL DESCRIPTION

4.84 See Figure 6–4 for the functional schematic diagram of the repeater test section. The function of the repeater test section is to provide an interface for many types of line and office repeaters, provide powering current, generate an interfering source signal used in the near end cross talk test, (NEXT), mix the interfering signal with a conventional PCM signal, apply an all ones signal to the idle side of the repeater under test, and to make available the PCM and fault locating signals for measurement by their respective receivers.

4.85 NEXT GENERATOR

4.86 The NEXT interference generator is located on Artline and NEXT board A11. The basic interference signal source is 9.238 MHz oscillator Q5 and Q7. Dividers U6, U7, and U8 result in frequencies of 770 kHz, 1.15 MHZ, and 1.54 MHz at select gates U9B, U9C, and U9A respectively. SYSTEM switch S1 selects one of the frequencies by applying ground to one of the select gates. The selected frequency is then filtered in one of the three bandpass filters. A second section of S1 applies the selected interfering signal to emitter follower Q6 that matches the input impedance of the NEXT attenuator.

4.87 INTERFERENCE MARGIN dB switch S2 selects one of 11 output levels from the attenuator. The level present at the input of T2 can be selected to be from 8 to 18 dB below an all ones signal at the input of the repeater to be tested. The output of T2 is then applied to the active artificial line.

4.88 If there is no plug inserted in either GENERATOR OUT jack J4 or J8 or MON jack J3, the PCM signal supplied by A13 is carried through the jacks. If there is no self test selected by SELF TEST switch S5, the PCM signal is applied to T1, located on repeater test board A13. The output of T1 is routed to A11 where it is linearly mixed with the interference signal at the input of the artificial line.

4.89 The artificial line simulates the inductance, capacitance, and resistance of varying lengths of span line ranging from a loss of 5 dB to 43 dB in 10 steps. The taps on the artificial line are selected by LINE LOSS dB switch S3 and applied to T1 that converts the single-ended signal to a balanced one before the signal is applied to repeater test board A13.

4.90 REPEATER TEST

4.91 The test signal at pins 3 and 4 and the all ones signal at J1 are routed to the two sides of the repeater under test via the multiple decks of REPEATER TEST switch S1 and relays K1 and K2. When testing side 1 of a 1 cable repeater, the test signal is applied through contacts of S1-D6, through isolation transformer T3, to side 1 in repeater test well A15. The output of side 1 is routed through isolation transformer T5, through contacts of S1-D2, and made available for measurement on A12.

The all ones signal for idle side 2, is routed through contacts of S1-D5, through the normally open contacts of operated relay K1, through contacts of S1-D3, and through isolation transformer T6. The output of side 2 is routed through isolation transformer T4, contacts of S1-D4, and through the normally closed contacts of not operated relay K2 where R2 provides the correct termination impedance. In a similar manner, S1 and relays K1 and K2 route the two signals to the appropriate sides of the repeater under test for side 2 of a 1 cable repeater and for a 2 cable repeater.

4.92 When SELF TEST switch S5, located on the front panel, is set of OFF, K4 is not operated and the fault locate pickoff coil output from the repeater under test is applied through the normally closed contacts of K4 to the fault locate receiver. In either self test mode, however, K4 operates and the input stage of the fault locate receiver is terminated by R31.

4.93 REPEATER POWERING

4.94 The function of the repeater powering section is to supply a constant current to the repeater under test. A meter circuit allows this current to be monitored and the voltage drop across the repeater internal power supply to be measured.

4.95 The current source is located on power supply assembly A14A1. The ac line voltage input is converted to a dc voltage in an ac-to-dc power supply. This dc voltage is used as the input to a variable constant current source. CURRENT ADJ potentiometer R1, located on the front panel, allows the current to be set within the range of 50 to 220 milliamperes. The powering loop is from the current source to the center tap of T3, through the internal power supply of the repeater under test, through the center tap of T4, and back to the current source. The current is monitored by measuring the voltage drop across R32 that is always in series with the current source.

4.96 Relay K3 senses whether the repeater under test is configured for looped or through powering. This is required so that the meter is connected in parallel with the internal power supply of the repeater regardless of the configuration. When the repeater is in the through configuration, K3 is included in the powering loop and it is operated. The negative side of the meter is now connected through the normally-open contacts of K3 to the center tap of T5. The positive side of the meter is connected to the center tap of T3. When the repeater is in the looped mode, K3 is removed from the current loop and it is not operated. The negative side of the meter is now connected to the center tap of T4 and the positive side to the center tap of T3.

4.97 LEAKAGE TEST

4.98 The function of the leakage test is to determine if the insulation resistance between the powering lead and the case of the repeater under test is capable of withstanding at least 200 Vdc without breaking down.

4.99 During testing within the test set, the repeater under test has its powering input lead connected to repeater ground, which is then connected to earth ground through the normally closed contacts of HV LEAKAGE switch S2. When S2 is pressed, the −200 Vdc power supply located on A14A1 is placed between the repeater ground and earth ground, which is also connected to the case of the repeater under test. Any leakage resistance present from repeater ground to earth ground (case) of the repeater under test, is now placed in series with R2 and the −200 Vdc power supply. As long as the leakage resistance is greater than approximately one megohm, there is not enough voltage dropped across R2 to fire the neon lamp in S2. If the leakage resistance is less, the lamp is lighted indicating that the repeater input powering lead cannot withstand 200 Vdc to the case.

4.100 **CLOCK ASSEMBLY A5 DETAILED CIRCUIT DESCRIPTION**

4.101 See Figure 6−12 for the schematic diagram of the clock assembly. The function of the clock assembly is to generate the basic clock signals used in the transmitters and receivers and also in clock recovery from the received signal.

4.102 CLOCK OSCILLATORS

4.103 Transistors Q4 through Q7 and their associated crystals form the basic clock oscillators. Capacitors C5 through C7 and C27 provide a limited range of frequency adjustment for calibration. Transistors Q1 through Q3 and Q8 decrease the rise times of the oscillator outputs. The 6.178 MHz output of Q8 is applied to a pair of tandem J-K flip flops connected to divide by four. The 1.544 MHz output is buffered by U7F and is designated FLØ. This is the basic clock signal used in the digital fault locate generator.

4.104 One of the three remaining oscillator outputs is selected for the 4Xϕ output by decoding the system select lines. As shown in Table 4−1, the line that is low selects the corresponding oscillator output. The selected frequency at the output of U1A is four times the desired bit rate. This is used by the clock recovery circuit and is also made available at pin D as 4Xϕ, which is used by the T148 generator. The 4Xϕ signal is also divided by four in U6A/B. The Q output of U6A is buffered by U7D and made available at pin 12 as CLOCK(X), which is eventually used by the transmit circuits.

4.105 CLOCK RECOVERY

4.106 The function of the clock recovery circuit is to synchronize the internal clock with the received data. The recovery circuit consists of U5A/B, U8, and U2A-C. Data at pin 17 is asynchronous with 4Xϕ, has a 50 percent duty cycle, and has a period that is one quarter that of 4Xϕ. As shown on Figure 4—2, the data can be anywhere from virtually in sync with 4Xϕ to 1/4Xϕ out of sync. J-K flip flop U5B registers the presence of logical ones in the data. Assuming that a logical one is present at the J input of U5B, the next high-to-low transition of $\overline{4X\phi}$ will trigger the flip flop. The high Q output of U5B conditions the J input of U5A so that the next high-to-low transition of $\overline{4X\phi}$ triggers U5A. Its high Q output conditions its own K input and the K input of U5B so that the next high-to-low 4Xϕ transition triggers both flip flops, returning them to their original state. The end result of this detection cycle has been to generate a low pulse at the $\overline{Q}$ output of U5B. This loads an eight-bit word into shift register U8. Secondly, a 25 percent duty cycle negative pulse is generated at the $\overline{Q}$ output of U5A. This second pulse is passed by U2B into the recovered clock bit stream and is designated CLOCK(R).

4.107 Thus for every logical one present in the data, a positive clock pulse is generated at the output of U2B. When the last logical one was detected, inputs A through H were loaded into U8. A and E are logical ones and the remaining are logical zeros. When the LD input goes high, U8 is enabled and starts to count 4Xϕ pulses. For each low-to-high transition of 4Xϕ, the A through H inputs previously loaded into U8 will shift one bit to the right. If the logical one in the data is immediately followed by a logical zero, the high E input will appear at the QH output after four 4Xϕ pulses. During this time, all three inputs of U2C are high. This forces its output low, which is passed by U2B to form a recovered clock pulse in the absence of a logical one in the data. Since strings of up to 14 logical zeros can occur in the data, U8 is connected in a recirculating mode. QH is connected to the serial input and since every fourth shift causes QH to go high because of E, the pattern originally loaded into U8 is continuously recycled. In this manner, synchronized clock pulses can be generated in the absence of logical ones for long periods of time.

4.108 Since the pulses appearing at the Q output of U5B are reclocked versions of the data, this output is used for the recovered T1 and T1C data, which is synchronous with the recovered clock. For T148, both positive and negative pulse streams are required. In this case, the asynchronous ± PULSES are reclocked by the Q output of U5B to generate T148 ± PULSES that are synchronous with the recovered clock.

4.109 TRANSMIT GENERATOR ASSEMBLY A2 DETAILED CIRCUIT DESCRIPTION

4.110 The transmit generator assembly is comprised of a QRSS signal generator, a single rail-to-double rail converter, an error inserter, and a repeater idle side generator. See Figure 6—14 for the schematic diagram.

4.111 QRSS GENERATOR

4.112 The actual QRSS signal generator is made up of 20-bit shift register U4, U8, and U12 and exclusive OR gates U14A/C. The Bell Standard quasi-random signal having a word length of 1,048,575 bits is created by returning bits 17 and 20 to the serial input of the shift register through exclusive OR gate U14C. Under normal conditions, U14A simply passes this to the serial input. The basic shift rate is contolled by CLK, which is a function of the system selected. The QRSS generator output is bit 20.

Table 4—1. Basic Clock Frequency Select Truth Table

$\overline{\text{T1 SEL}}$	$\overline{\text{T148 SEL}}$	$\overline{\text{T1C SEL}}$	4XΦ FREQ	CLOCK(X) FREQ
L	H	H	6.178 MHz	1.544 MHz
H	L	H	9.48 MHz	2.37 MHz
H	H	L	12.608 MHz	3.152 MHz

4.113 QRSS specifications do not allow more than 14 consecutive zeros in the transmitted bit stream. During normal operation, it is possible for the QRSS generator to produce up to 19 consecutive zeros. A 15 zero detector looks at the 15 bits preceding the output and when it detects all zeros, it stuffs logical ones into the output until the 15 zero condition no longer exists. The 15 zero detector consists of U13A, U9A-C, U5B-D, U10B, U11A/B, and U14D. When 15 zeros are detected, the output of U10B goes high, which is inverted by U11A. If T1C has not been selected, T1C SEL is low and the output of U11A is high. Since bit 20 (U4-QD) is low during this time, the output of exclusive OR gate U14D will be high (logical one) as long as the 15 zero condition lasts. Fifteen zero suppression is not used when T1C is selected. During this time, T1C SEL is high and U11A is inhibited so that its output is held permanently low thus inhibiting the 15 zero detector.

4.114 When power is first applied to the unit, it is possible that the shift registers could have all low outputs. With no logical ones to shift into the serial input, all outputs would remain zeros permanently and normal opertion would never begin. This condition is detected by a combination of the 15 zero detector previously described and an additional five zero detector comprised of U13B/C. If 20 zeros are detected, all of the inputs of U10A are high and its output goes high. The high output of U10A is passed by U14A and appears at the serial input of U12. This guarantees that 17 bits later a logical one will appear at bit 17, be fed back, and get normal QRSS operation started.

4.115 The QRSS bit stream present at the output of U14D is inverted by U1F and applied to controlled gate U2B. Table 4–2 shows that when function switch A12S1 is set to any position demanding a QRSS signal or to XMIT ERRORS, the output of U2C is high and U2B passes the QRSS signal. When any of the measure functions or the all ones funtion is selected, both inputs of U2C are high. The low output of U2C inhibits U2B and the QRSS signal is blocked. The signals for these functions are generated by other circuits and the QRSS signal is not required. The $\overline{\text{XMT ERRORS}}$ input is also inverted by U1A and becomes the ERROR SEL line used to activate the error timer located on A5.

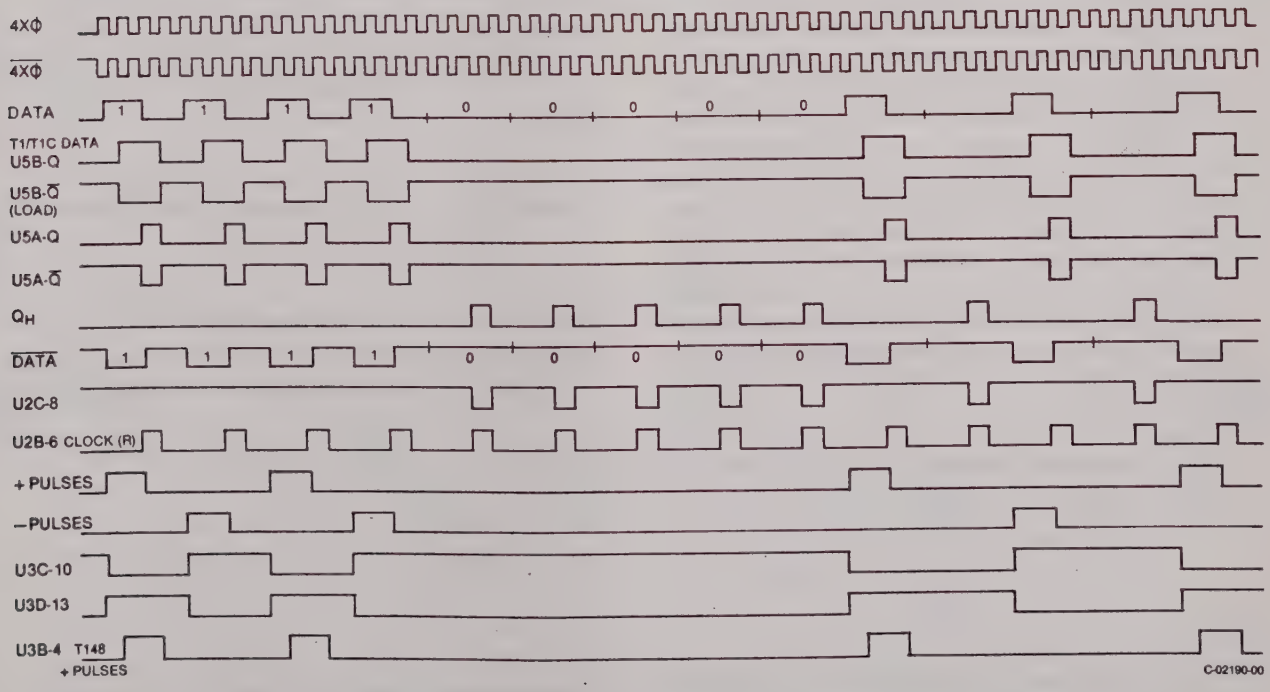

Figure 4–2. Clock Recovery Timing Diagram

Table 4—2. QRSS Generator Output Gate Enable/Inhibit Truth Table

A12S1 FUNCTION	$\overline{\text{QRSS}}$	$\overline{\text{XMIT}}$ $\overline{\text{ERR}}$	U2B
ANY QRSS	L	H	ENABLE
XMIT ERRORS	H	L	ENABLE
ANY MEAS OR ALL 1'S	H	H	INHIBIT

4.116 SINGLE RAIL-TO-DOUBLE RAIL CONVERTER

4.117 The function of the single rail-to-double rail converter is to transform the QRSS signal that exists in a single rail, 100 percent duty cycle format into two bit streams that contain alternate logical ones present in the original bit stream. The circuit is comprised of U7A and U3A/B. The QRSS signal is present at the output of U2B for all QRSS and ERRORS functions and for all three bit rates. Whenever the T148 bit rate is selected, the output of U2A is low and both U3A/B are inhibited. See Table 4—3. In this case, the QRSS signal is applied to the T148 generator located on A6. For the T1 and the T1C bit rates, the QRSS signal is processed as follows. See Figure 4—3 for the timing diagram. Inputs 2 and 12 of U3A/B are high. Every time a logical one appears in the QRSS bit stream, J-K flip flop U7A toggles. This alternately enables U3A and U3B. The only time that all inputs to either of these gates are high is during the half cycle of CLK immediately following the registration of a logical one. At this time, the output of either U3A or U3B goes low for one half clock cycle. The outputs of U3A and U3B are bit streams containing alternate logical ones. When no errors are being requested, U6A is cleared and its low Q output allows CLK to be passed by U5A and inverted by U1E.

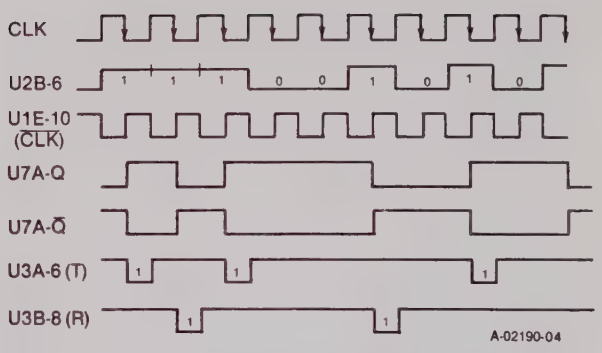

Figure 4—3. Single Rail-To-Double Rail Converter Timing Diagram

4.118 When the all ones format is requested, the output of U2B is held high. See Figure 4—4 for the timing diagram. Thus U7A toggles on every high-to-low transition of CLK. In this manner either the output of U3A or U3B goes low for alternate $\overline{\text{CLK}}$ cycles and the all ones signal is generated.

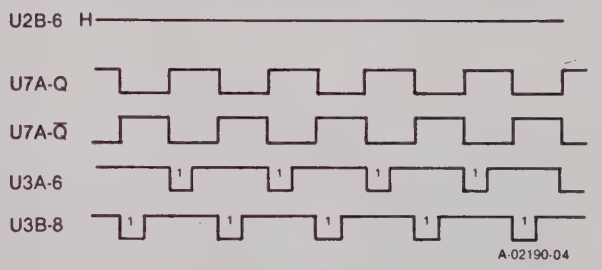

Figure 4—4. All Ones Generator Timing Diagram

4.119 ERROR INSERTER

4.120 The function of the error inserter is to force one bipolar violation approximately every two-thirds of a second. For T1 and T1C and when errors are requested,

Table 4—3. QRSS, All Ones, and Errors Output Gates Enable/Inhibit Truth Table

A12S1 FUNCTION	A11S1 SYSTEM	$\overline{\text{M SEL}}$	$\overline{\text{T148 SEL}}$	$\overline{\text{1111}}$	U3A/B
ANY QRSS OR OR XMT ERRORS	T1 or T1C	H	H	L	ENABLE
ALL 1'S	X	H	X	L	ENABLE
ANY MEAS	X	L	X	H	INHIBIT
QRSS, MEAS, OR XMT ERRORS	T148	†	L	H	INHIBIT

†: L for MEAS otherwise H.
X: Irrelevant.

ERROR TIMER input at pin E goes low approximately every two-thirds of a second. At T1 bit rates, this corresponds to a bit error rate of 10^6. A bipolar violation will be generated only when two consecutive logical ones appear in the bit stream at the output of U2B.

4.121 Before errors are requested, the starting conditions are as follows. Flip flops U7B and U6A/B are all in the cleared state with their Q outputs low. This enables U5A so that it can pass CLK to double rail gates U3A/B. As shown on Figure 4—5, the error request sets U7B and its Q output goes high. At the next low-to-high CLK transition and after the output of U2B goes high, i.e., a logical one is present, U6A is set and its Q output goes high. The next low-to-high $\overline{CLK}$ transition sets U6B and its Q output goes low. This is used to clear U7B, acknowledging that all of the conditions required to generate an error have occurred. With the Q output of U7B low, U6A is cleared on the next low-to-high CLK transition. Its Q output goes low and the next low-to-high $\overline{CLK}$ transition clears U6B and its Q output goes low. This now frees U7B so that it can respond to the next error request.

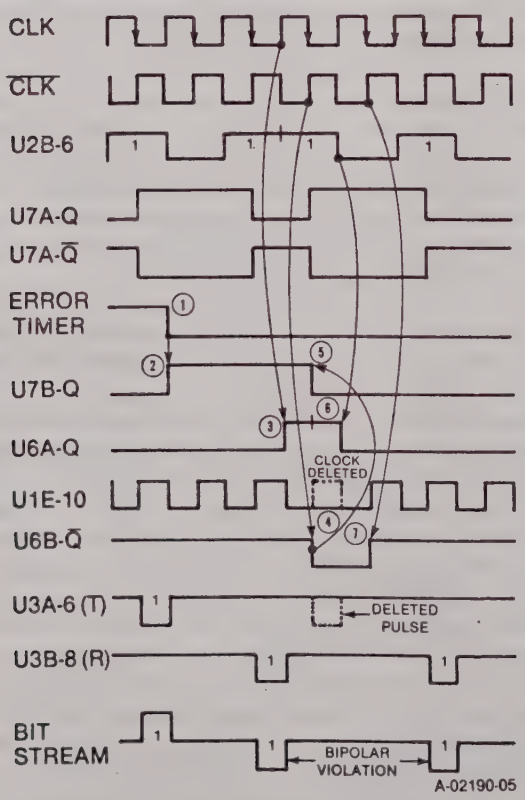

Figure 4—5. Error Inserter Timing Diagram

4.122 The total effect of the three flip flops just described has been to inhibit U5A long enough to delete one CLK pulse from arriving at U3A/B during the time a logical one is present. This deletes a logical one at the output of either U3A or U3B and results in two consecutive logical ones at one or the other of these gates. This fits the definition of a bipolar violation.

4.123 REPEATER IDLE SIDE ALL ONES GENERATOR

4.124 The function of the repeater idle side all ones generator is to continuously generate a stream of logical ones. This signal is used by the idle side of a repeater in the test well to prevent oscillations.

4.125 The input to the all ones generator is the basic transmit clock signal CLOCK(X). This is applied to U15B, a flip flop connected to toggle on each positive transition of CLOCK(X). This divides the clock by a factor of two. Application of the Q and $\overline{Q}$ outputs, along with the basic clock signal, results in alternate positive pulses, having a 25 percent duty cycle, to appear at the output of U11C and U11D. These signals are applied to transformer drivers Q1 and Q2. Emitter follower-type voltage regulator Q3 generates a voltage that is applied to the center tap of transformer T1. The level of this voltage is adjusted so that the peak-to-peak signal level at the secondary is six volts. The two positive pulse streams cause Q1 and Q2 to alternately conduct and ground alternate ends of the transformer. Thus current reverses through the transformer on alternate pulses. An artificial line designed to have 24 dB of loss at 772 kHz is connected between the two halves of T1. The balanced output of T1 is then applied to the idle side of the repeater under test.

4.126 DIGITAL FAULT LOCATE GENERATOR ASSEMBLY A8 DETAILED CIRCUIT DESCRIPTION

4.127 See Figure 6—16 for the schematic diagram. The function of the digital fault locate generator is to generate one of twelve available fault locate audio-frequency signals and use this signal to impart an audio component to the digital fault locate signal. The assembly is comprised basically of an audio generator and a pattern generator.

4.128 AUDIO GENERATOR

4.129 The audio generator is a frequency synthesizer that uses a programmable counter to divide the basic 1.544 MHz input down to the desired audio-frequency signal. $\overline{FLS1}$ through $\overline{FLS12}$ are the select lines controlled by LINE FILTER switch A10S2. Only the selected line is low while all of the others are pulled high through resistors located on another assembly. Some additional decoding is provided by U1A-D which are then used to form five-bit address codes for PROMS U5 and U10.

The relationship between the filter code selected and the PROM address is shown in Table 4—4.

Table 4—4. Fault Locate Audio Generator PROM Addresses

FILTER SELECTED	ADDRESS CODE									
	U5					U10				
	A	B	C	D	E	A	B	C	D	E
A	L	H	H	L	L	H	H	H	L	L
B	H	L	H	L	L	H	H	H	L	L
C	H	H	L	L	L	H	H	H	L	L
D	H	H	H	H	L	H	H	H	L	L
E	H	H	H	L	H	H	H	H	L	L
F	H	H	H	H	H	H	H	H	L	L
G	H	H	H	L	L	L	H	H	L	L
H	H	H	H	L	L	H	L	H	L	L
J	H	H	H	L	L	H	H	L	L	L
K	H	H	H	L	L	H	H	H	H	L
L	H	H	H	L	L	H	H	H	L	H
M	H	H	H	L	L	H	H	H	H	H

4.130 Binary counters U19 and U20 together form an eight-bit programmable counter. As shown in Table 4-5, the 12 filter codes (A through M) represent audio frequencies ranging from 832 Hz to 3017 Hz. For a counter output frequency that is eight times the audio frequency, division ratios ranging from 232 to 64, respectively, are required. As an example, suppose it is desired to generate the audio frequency associated with filter code A. The final frequency is 832 Hz and the output of the counter must be 6655 Hz. Starting with a 1.544-MHz input, a division ratio (N) of 232 is required. This is obtained by presetting the counter to 24 and then counting up until it overflows at its maximum count of 256. By ANDing the carry outs of U19 and U20, along with the basic clock in U15C, a load pulse is generated once per division cycle. This pulse is the counter output as well as the load pulse. Figure 4—6 shows the timing of the two carry lines, the FLØ clock, and the load pulse.

4.131 The X8f_{FL} output of U15C is applied to one shots U2A/B and to binary counter U11. The output of U2B is a series of 600-nanosecond pulses at the same frequency as the input. Retriggering of the one shot is prevented by connecting the $\overline{Q}$ output to the B input. Thus any multiple edges are removed and the FLD1S signal is taken at the Q output.

4.132 The X8f_{FL} output of U15C is also applied to binary counter U11 and to one shot U2A. The QB, QC, and QD outputs of U11 are at 2X, 4X and 1X of the desired output, f_{FL}. The output of U2A is a series of negative, 450-nanosecond pulses used to reclock the outputs of U11 through clocked flip flops in U6. The reclocking removes any multiple edges that might be present. The outputs; designated FLA, FLB, and FLC; are then used in the fault locate receiver. FLC is also used by the fault locate pattern generator.

4.133 PULSE PERIOD GENERATOR

4.134 The function of the pulse period generator is to automatically step the pattern generator from pulse period 11 to pulse period 4 during automatic operation. It also generates pulse period 4 permanently as a reference and stops the pulse period wherever it happens to be during the hold mode. The generator is comprised of a pulse period stepping oscillator and a pulse period counter.

4.135 Pulse period stepping oscillator U13 is connected as an astable multivibrator. The period of oscillation is controlled by R30, R12, R14, and C11. Potentiometer R30 sets the period. It is normally set so that the period at Q is 2.5 seconds. For the reference and auto functions, the $\overline{\text{HOLD}}$ input is high and U17A toggles to divide the pulse period by two.

4.136 When $\overline{\text{RESET}}$ is low during the reference time, the output of U18F is high and pulse period counter U4 is held in the reset condition. See Figure 4—7. This forces the QB, QC, and QD outputs of the counter low. This is the condition required by the pulse period zero counter to generate pulse period 11. As soon as the automatic stepping mode is selected, $\overline{\text{RESET}}$ goes high and the counter reset goes low, freeing the counter. The next clock transition at U4-1 advances the counter. Successive clock pulses are counted until the count of seven is reached. At this time, QB, QC, and QD are all high. This condition is detected by U21B and its output goes low. The J and the K inputs of U17A are now both low and it can no longer toggle. With no inputs, U4 stops counting and its outputs remain in the state that corresponds to pulse period 4. This condition remains until the front panel PULSE PERIOD switch is again set to REF and then to AUTO. Any time this switch is set to HOLD, $\overline{\text{HOLD}}$ is low, U17A is inhibited, and counting immediately halts. This holds the pulse period at its present number for as long as the switch is in HOLD.

Table 4—5. Fault Locate Audio Generator Preset Codes and Division Ratios

FL FILTER CODE	f_{FL} (Hz)	U19-U20 PRESET CODE 128	64	32	16	8	4	2	1	DECIMAL PRESET	DIVISION RATIO N*	8x f_{FL} (Hz)
A	832	L	L	L	H	H	L	L	L	24	232	6655
B	928	L	L	H	H	L	L	L	L	48	208	7423
C	1049	L	H	L	L	H	L	L	L	72	184	8391
D	1206	L	H	H	L	L	L	L	L	96	160	9650
E	1340	L	H	H	H	L	L	L	L	112	144	10722
F	1508	H	L	L	L	L	L	L	L	128	128	12063
G	1723	H	L	L	H	L	L	L	L	144	112	13786
H	2010	H	L	H	L	L	L	L	L	160	96	16083
J	2193	H	L	H	L	H	L	L	L	168	88	17545
K	2413	H	L	H	H	L	L	L	L	176	80	19300
L	2681	H	L	H	H	H	L	L	L	184	72	21444
M	3017	H	H	L	L	L	L	L	L	192	64	24125

* N = (255 − PRESET) + 1

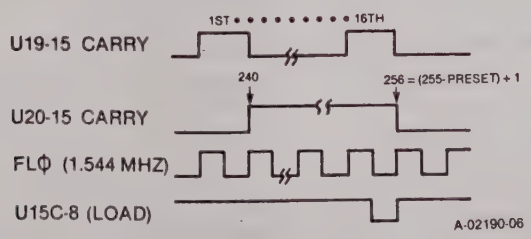

Figure 4—6. Fault Locate Audio Generator Preset Counter Load Pulse Timing Diagram

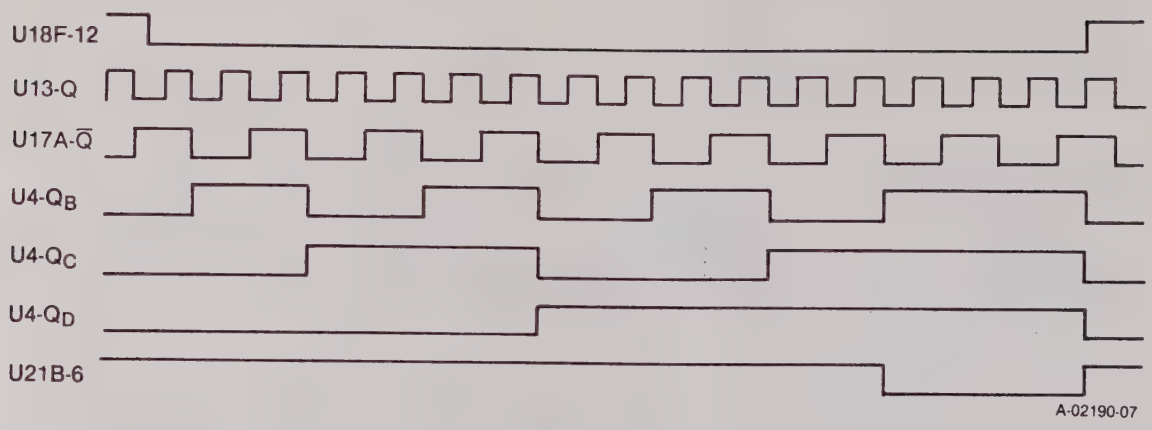

Figure 4—7. Pulse Period Counter Timing Diagram

4.137 Visual pulse period indication is provided by BCD-to-decimal decoder/driver U9. The eight outputs are connected to the PULSE PERIOD LED indicators through current-limiting resistors R4 through R11. A lamp test mode is also provided. when the front panel LAMP TEST pushbutton is pressed, LAMP TEST goes high. This is inverted by drivers U14A-F and U18A/B, which are wire ORed with the U9 outputs.

4.138 TRIAD GENERATOR/PULSE PERIOD ZERO COUNTER

4.139 The function of the triad generator/pulse period zero counter is to generate a three-pulse triad followed by a variable number of zeros determined by the pulse period in use.

4.140 The triad generator is comprised of two-bit binary counter U3A/B, gates U7B/D, and inverter U7A. The sole purpose of this circuit is to count three CLOCK(X) pulses and shut itself off. As shown on Figure 4—8, the most convenient starting point is to assume that the QD output of U8 has just generated a positive pulse. This is inverted by U7A and clears both U3A and U3B. With both Q outputs low, the U7D output goes high to enable clock gate U7B. During the first two counts, one of the U3A/B Q outputs will be low. This keeps the clock enabled. At the count of three however, both Q outputs go high and the output of U7D goes low to inhibit U7B and counting halts. This state continues while the zero counter is counting the required number of zeros. The outputs of the triad generator are then applied to the MEAS 1/2/3 generator.

4.141 The purpose of the pulse period zero counter is to insert the required number of zeros between adjacent triads. The number required is always three less than the pulse period number. See Table 4—6. As an example, for pulse period five the counter is preset to six and the resulting number of zeros is two. This case is also shown on the timing diagram. Assuming that the triad generator is in the process of counting three pulses, the U21A $\overline{Q}$ output is low. This loads the decimal number six (supplied by U4) into counter U8. Counting is inhibited as long as the load line is low. Now assume that the triad generator has just counted the third pulse and the D input of U12A is low. On the next positive transition of the U12A clock input, the $\overline{Q}$ output goes high. U8 is now placed in the count mode and counts the required two pulses being used in this example. When the second pulse is counted, the counter has actually reached a count of eight and the QD output goes high thus restarting the triad/zero cycle. The QD output is also used by the MEAS 1/2/3 generator.

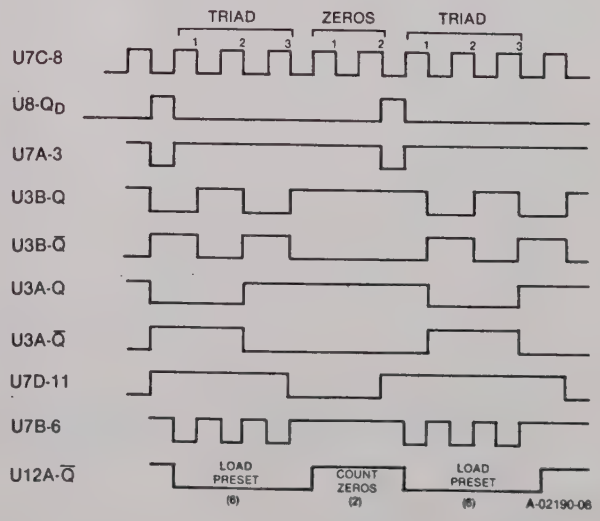

Figure 4—8. Triad Generator/Zero Counter Timing Diagram

Table 4—6. Relationship Between Pulse Period, Counter Preset, and Number of Zeros

PULSE PERIOD	11	10	9	8	7	6	5	4
COUNTER PRESET	0	1	2	3	4	5	6	7
NUMBER ZEROS	8	7	6	5	4	3	2	1

4.142 MEASURE 1/2/3 PATTERN GENERATOR

4.143 The function of the measure 1/2/3 pattern generator is to generate strings of either positive triads, negative triads, or normal bipolar pulses in the appropriate combinations. A complete discussion of the measure 1 function will serve as the basis for lesser discussions of the very similar measure 2 and measure 3 functions. Complete timing diagrams are provided for each function, however.

4.144 When measure 1 is selected, $\overline{\text{MEAS 1}}$ is low and both $\overline{\text{MEAS 2}}$ and $\overline{\text{MEAS 3}}$ are high. The basic inputs to the circuit are CLOCK(X) and FLC. See Figure 4—9. The clock frequency is that of the system selected and the FLC audio frequency depends on the fault locate filter code selected. This varies from 832 Hz to 3017 Hz. With $\overline{\text{MEAS 1}}$ low, U22A is enabled and its high output enables one input each of U22B and U22C.

4.145 Assuming that the first half cycle of the FLC signal is high, the next positive transition of the clock forces the U12B Q output high and its $\overline{\text{Q}}$ output low. The low output inhibits U21A and the high output, along with the high $\overline{\text{MEAS 3}}$ line, enables two of the U21C inputs. Immediately preceding each triad at U7B-6 is a positive pulse supplied by zero counter U8. This pulse is passed by U21C and the leading edge presets the U17B Q output high. This ensures that the first pulse of a positive triad is indeed positive. Since J-K flip flop U17B is configured to toggle on the clock input, the three pulses supplied by the triad generator cause the flip flop to change state three times per triad. The two inputs of U16B, supplied by U16A/C, are low and the triad pulses supplied by U7B are inverted before being used to clock U17B. Combining the Q and $\overline{\text{Q}}$ outputs with the output of U16B in gates U22B/C, a double rail output is produced. The first pulse of the positive triad appears as a negative pulse at the output of U22B. The next pulse supplied by the zero counter presets U17B again and the cycle continues as long as FLC remains high.

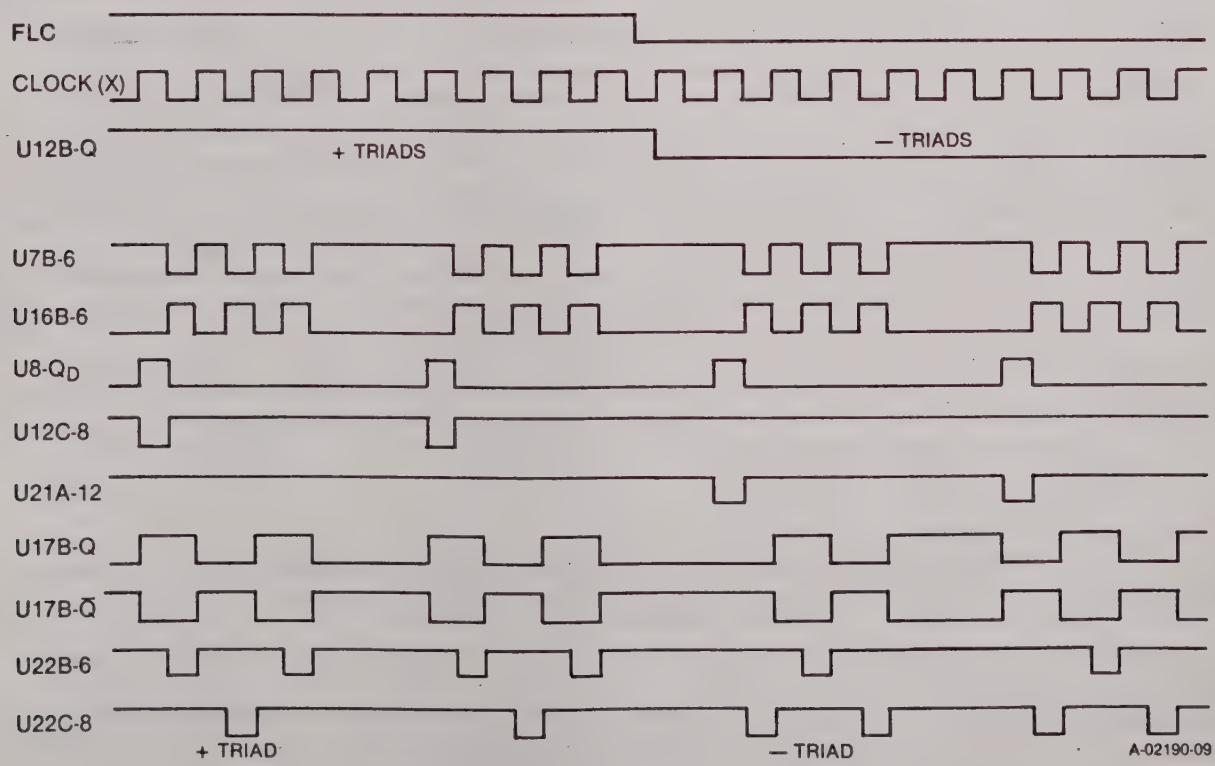

Figure 4—9. Measure 1 Pattern Generator Timing Diagram

4.146 The next time the U12B clock goes high after FLC goes low, the outputs of U12B change. The low Q output inhibits U21C while the high $\overline{Q}$ output enables the second input of U21A. The operation is identical to that for positive triads with the exception that U17B is cleared at the beginning of each triad through U21A.

4.147 When measure 2 is selected, the output consists of positive triads followed by normal bipolar pairs, all of which follow the audio rate of FLC. See Figure 4—10. For the positive half of FLC, positive triads are generated exactly as in measure 1. When U12B changes after FLC goes low, U16C is inhibited and two of the inputs of U16A are enabled. The $\overline{Q}$ output of U3A is high during the first two pulses supplied by U7B but goes low before the third pulse. All three inputs of U16C are now low and its high output inhibits U16B. The third triad pulse supplied by U7B is now blocked. The result of this is that U17B is clocked only twice and the decoding supplied by U22B/C produces just two pulses, which will eventually result in a bipolar pair. This continues as long as FLC is low.

4.148 The measure 3 signal consists of negative triads followed by bipolar pulses. See Figure 4—11. These are generated when FLC is low and high respectively. The negative triads are generated exactly as described for measure 1. The bipolar pulses are generated by inhibiting the third pulse from the triad generator. This is done with the high output of U16A.

4.149 When either measure 1/2/3 is selected, the output of U22A goes high. This is inverted by U18C for use by the QRSS transmitter.

4.150 T148 GENERATOR ASSEMBLY A6 DETAILED CIRCUIT DESCRIPTION

4.151 See Figure 6—18 for the schematic diagram of the T148 generator. The function of the T148 generator is to convert a QRSS binary bit stream into a ternary bit stream in accordance with a unique encoding scheme and to insert both logical and disparity errors upon demand. The four major functional sections of the

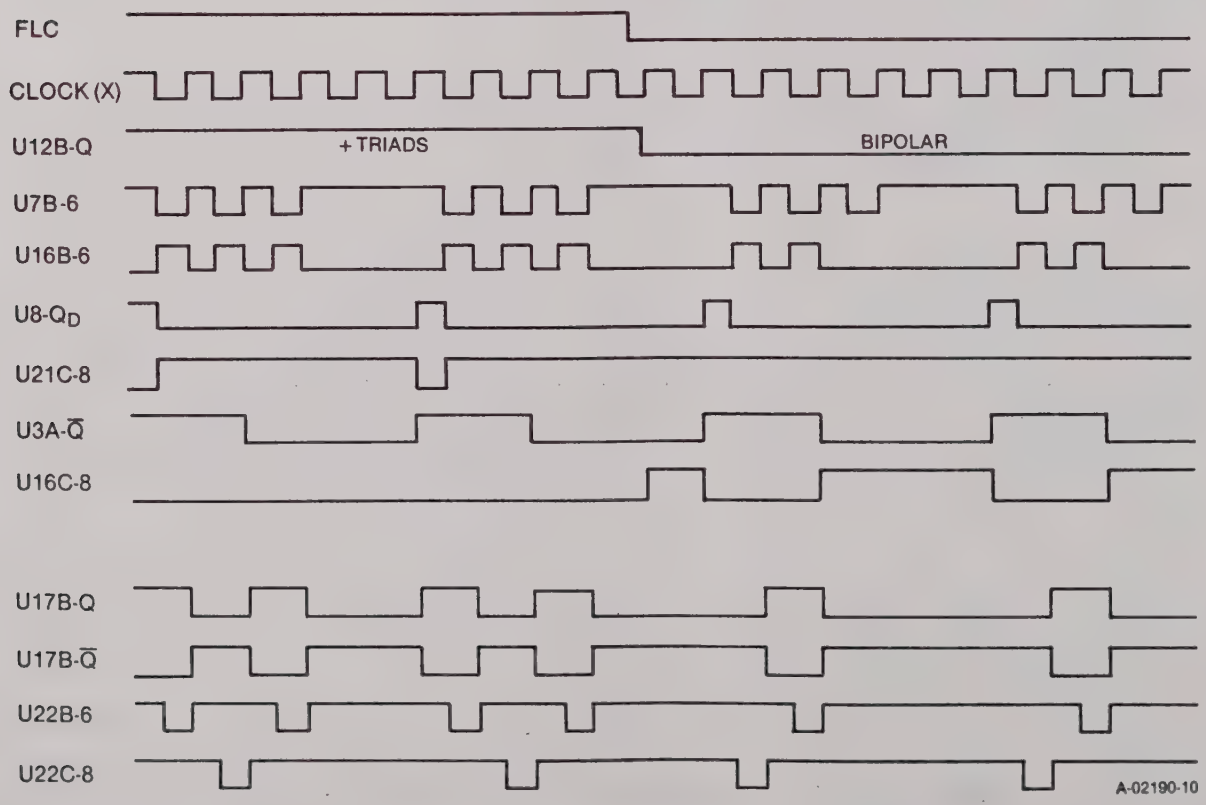

Figure 4—10. Measure 2 Pattern Generator Timing Diagram

generator are an output time slot generator, a 4 binary-to-3 ternary converter, a logical error generator, and a disparity generator.

4.152 OUTPUT TIME SLOT GENERATOR

4.153 The function of the output time slot generator is to generate timing waveforms that are used in the 4 binary-to-3 ternary converter. Figure 4—12 is the timing diagram that shows the various signals generated by the timing generator. The generator basically consists of a series of dividers interconnected by decoding gates to produce the desired signal phasing. A divide by four counter is formed by U6A/B interconnected in such a manner that the frequencies of A and B are identical but displaced one quarter time slot. Since the 4X0 input is at four times the desired T148 bit rate, all of the A and B signals developed by the generator are at the T148 rate. Flip flops U2A/B and their associated gates are connected so that the C outputs are at one twelveth the input clock rate and the D outputs at one sixth. The D signal is reclocked by U3B to alter its phase. This D1 signal and C are applied to U14D and generate the basic LOAD signal.

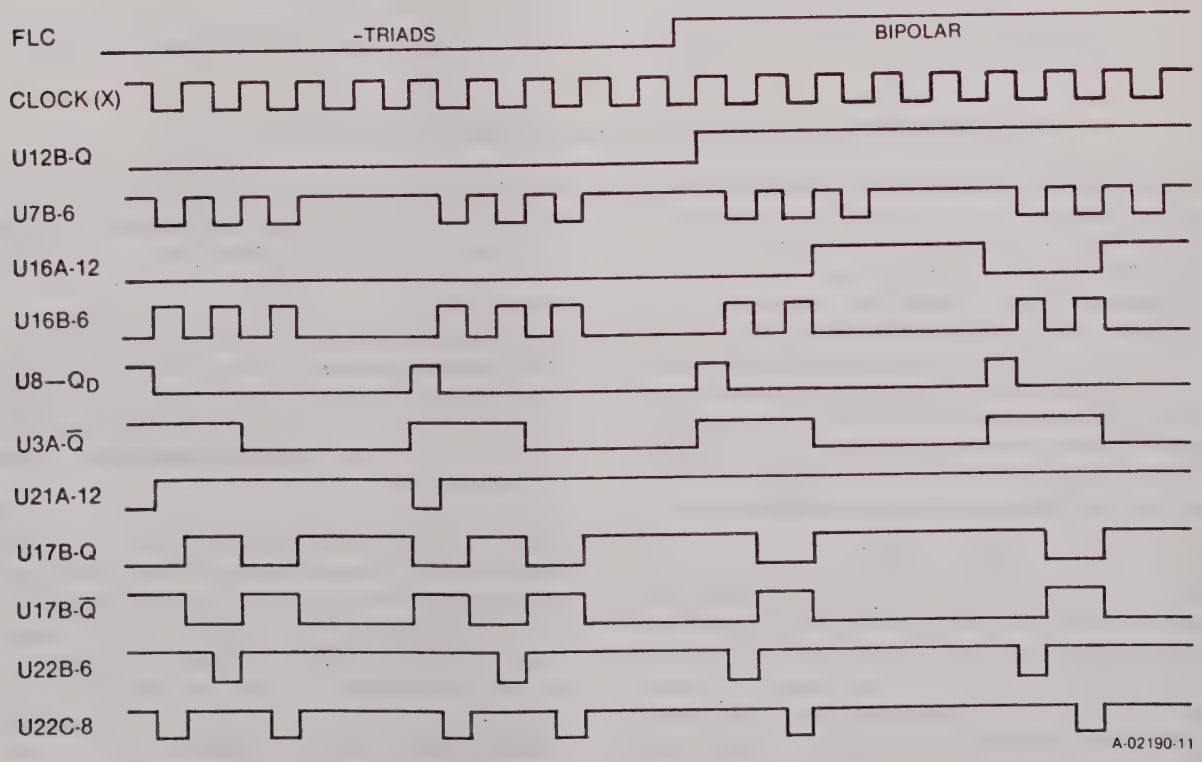

Figure 4—11. Measure 3 Pattern Generator Timing Diagram

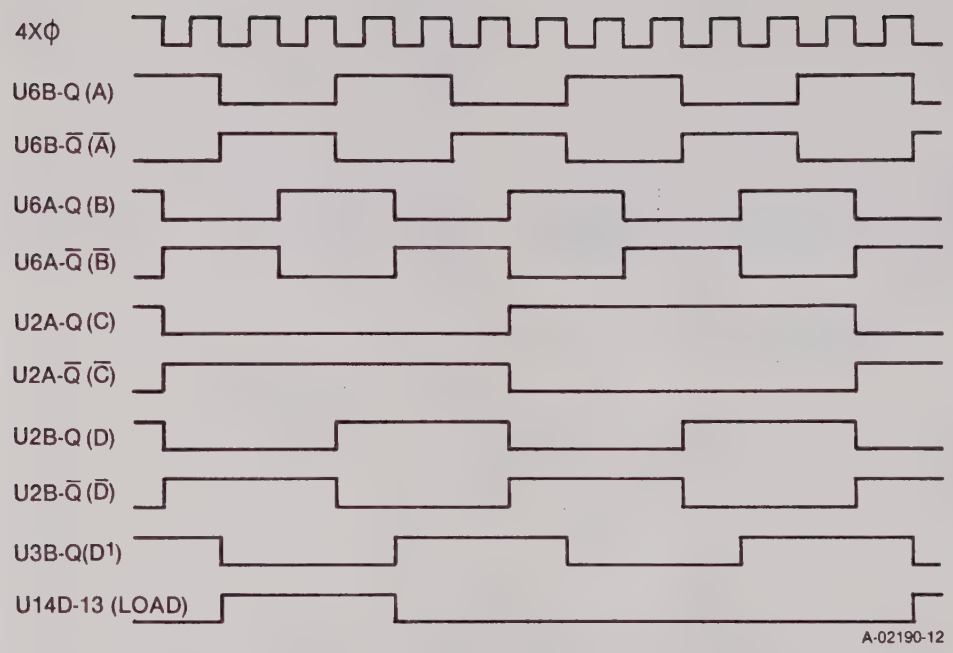

Figure 4—12. Output Time Slot Generator Timing Diagram

4.154 4 BINARY-TO-3 TERNARY CONVERTER

4.155 The basic function of the 4 binary-to-3 ternary converter is to take 4-bit words supplied by the QRSS generator located on A2 and convert them to 3-bit words according to a predetermined encoding scheme. The timing and sequence diagram shown on Figure 4—13 depicts the steps in the conversion sequence. All of the waveforms generated or used by the converter are synchronous with 4Xϕ, the source of all waveforms generated by the output time slot generator. In addition, the T148 XMT DATA input is derived from the T148 XMT CLOCK signal.

4.156 The basic 4Xϕ clock input and the CLEAR signal generated by the time slot generator are used by input clock counter U17 to create the T148 XMT CLOCK. The LOAD signal is inverted by U13A to form the CLEAR line used by U3A and U17. The low level clears both devices and no further operation can occur until this line returns high. After the clear line goes high, U17 starts counting the clock input. Since QD is low during the first eight counts, the output of U14C is an inverted replica of QA. This is applied to the U3A/D input and is reclocked by $\overline{4X\phi}$. The T148 XMT CLOCK signal present at the output of U3A consists of four clock cycles at twice the T148 bit rate and a low period equal to two cycles.

4.157 Since the T148 XMT DATA input applied to the serial input of shift register U5 is derived directly from the T148 XMT CLOCK, it is formatted into 4-bit words separated by a dead period. When no errors are being demanded, the U16A Q output is high and the T148 XMT DATA signal is applied to the shift register SERIAL INPUT. The duty cycle of the T148 XMT DATA input is 100 percent and each of the four bits is shifted into U5 by the positive edge of the T148 XMT CLOCK. After the four shifts, the logical level of the four data bits are present at the QA and QD outputs of U5. This represents the first step in the conversion process. The bits are now frozen in time and are further manipulated.

4.158 The U5 QA-QD outputs represent the four most-significant address bits for PROM U10. A fifth least-significant bit is supplied by disparity counter U8. The function of this bit is described as part of the encoding scheme. With a five-bit address, 32 different locations can be called up from the PROM. Each of these locations contains two, three-bit words that form the basis for the tip and ring T148 outputs.

4.159 After a short interval to allow the PROM output data to settle, the positive LOAD gate allows the three-bit words to enter shift registers U18 and U19. At the first negative transition of $\overline{B}$, the A through C shift register inputs appear at the QA through QC outputs. Since only the QC outputs are used, the first of the three bits is now present at the QC output. These bits are applied to reclocking gates U9A/B that are enabled by the low T148 ENABLE input line. The bits are

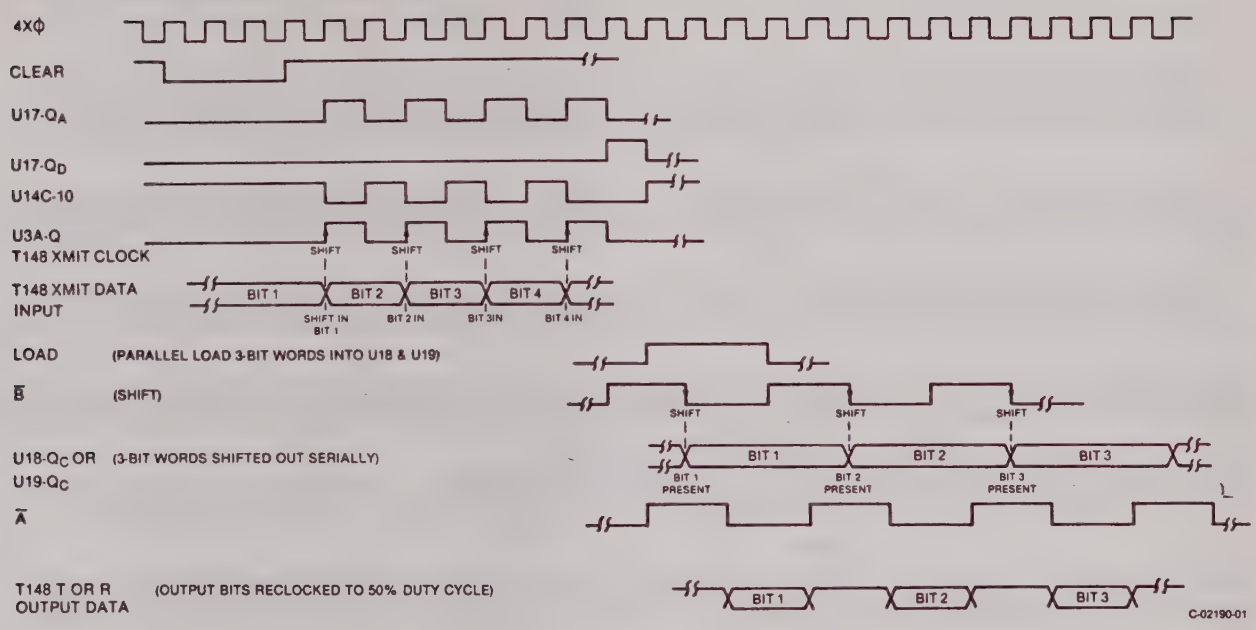

Figure 4—13. 4 Binary-To-3 Ternary Converter Sequence And Timing Diagram

reclocked by $\overline{A}$ to provide output bits that have a 50 percent duty cycle. After further inversions by U4F and U4A, the tip and ring data for the first bit is available at pins 16 and 17.

4.160 The next negative transition of $\overline{B}$ shifts the B inputs to the QC outputs of U18 and U19. These bits are reclocked and then the third bit is shifted out. After additional reclocking, the conversion of this three-bit word is now complete and the cycle repeats.

4.161 The T148 encoding scheme makes a distinction between a positive logical one and a negative logical one. It is this distinction that makes it possible to encode a four-bit binary word into a three-bit ternary word. Unlike the alternate-mark-inversion format of the T1 and T1C systems, the T148 system permits adjacent ones to be of the same polarity. To keep the dc component on the span line to a minimum, the long-term average of positive logical ones should be as close as possible to the negative logical ones. The long-term difference between positive ones and negative ones can be kept track of very conveniently in an up-down counter. The positive ones increment the counter and the negative ones decrement it. The scheme does allow an excess of either positive or negative ones within the range of one to four at any point in time. This difference is called disparity and is the second key element in the T148 encoding scheme.

4.162 The information contained in Table 4—7 defines the operation of disparity counter U8. When the unit is first powered up, the counter state is indeterminate. The counter, at this time, can be anywhere within the range of 0 to 15, which represents disparity values ranging from −8 to +8 respectively. For discussion purposes, assume that the disparity at power up is +8. This condition causes the QD output to be high. This is the least-significant bit (A) of the five-bit address for PROM U10. As shown in Table 4—8, whenever this bit is high, the PROM word selected always has a word disparity that is either negative or zero. In this case, the next word to be encoded will have a word disparity that will reduce the long-term disparity magnitude, or at least not increase it. Assuming that a word is selected that has a word disparity of −3, the counter will be decremented three counts. The net result will be a counter disparity of +5. The QD bit remains high and another word is encoded that has a negative or zero word disparity. Assuming again that the selected word disparity is −3, the counter will show a disparity of +2 after being decremented. Again either a negative or zero disparity word will be selected. Assuming the selected word has a disparity of −2, the final counter state will be −1. The long-term disparity has now changed from positive to negative and the next word selected will either have a word disparity that is positive or zero. This is a result of a low QD output. Now that the disparity counter is within the allowable range of

eight states, it can never again exceed the boundaries of −4 to +4. The long-term disparity will, in general, bounce back and forth from negative to positive. In this manner, the disparity history determines the state of QD, which is then used to select a word that will either reduce or cause no change in the disparity magnitude.

Table 4—7. Disparity Counter U8 Truth Table

DECIMAL COUNT	DISPARITY	OUTPUTS				
		Q_D	Q_C	Q_B	Q_A	
15	+8	H	H	H	H	NOT ALLOWED AFTER START UP
14	+7	H	H	H	L	
13	+6	H	H	L	H	
12	+5	H	H	L	L	
11	+4	H	L	H	H	8 ALLOWABLE OPERATING STATES
10	+3	H	L	H	L	
9	+2	H	L	L	H	
8	+1	H	L	L	L	
7	−1	L	H	H	H	
6	−2	L	H	H	L	
5	−3	L	H	L	H	
4	−4	L	H	L	L	
3	−5	L	L	H	H	NOT ALLOWED AFTER START UP
2	−6	L	L	H	L	
1	−7	L	L	L	H	
0	−8	L	L	L	L	

Table 4—8. 4 Binary-To-3 Ternary Encoding and Disparity Truth Table

ADDRESS CODE FROM U5	DISP. BIT	LOCA-TION	TIP WORD	RING WORD	TIP OUT	RING OUT	COMBINED WORD (T-R)	WORD DISPARITY
L L L L	L	0	H L L	L H H	0 +1 +1	−1 0 0	−1 +1 +1	+1
L L L L	H	1	H L H	L H L	0 +1 0	−1 0 −1	−1 +1 −1	−1
L L L H	L	2	L H H	H H L	+1 0 0	0 0 −1	+1 0 −1	0
L L L H	H	3	L H H	H H L	+1 0 0	0 0 −1	+1 0 −1	0
L L H L	L	4	H H L	H L H	0 0 +1	0 −1 0	0 −1 +1	0
L L H L	H	5	H H L	H L H	0 0 +1	0 −1 0	0 −1 +1	0
L L H H	L	6	L H H	H L H	+1 0 0	0 −1 0	+1 −1 0	0
L L H H	H	7	L H H	H L H	+1 0 0	0 −1 0	+1 −1 0	0
L H L L	L	8	H H L	L H H	0 0 +1	−1 0 0	−1 0 +1	0
L H L L	H	9	H H L	L H H	0 0 +1	−1 0 0	−1 0 +1	0
L H L H	L	10	H L H	H H L	0 +1 0	0 0 −1	0 +1 −1	0
L H L H	H	11	H L H	H H L	0 +1 0	0 0 −1	0 +1 −1	0
L H H L	L	12	L H L	H L H	+1 0 +1	0 −1 0	+1 −1 +1	+1
L H H L	H	13	H H L	L L H	0 0 +1	−1 −1 0	−1 −1 +1	−1
L H H H	L	14	L L H	H H L	+1 +1 0	0 0 −1	+1 +1 −1	+1
L H H H	H	15	L H H	H L L	+1 0 0	0 −1 −1	+1 −1 −1	−1
H L L L	L	16	H H L	H H H	0 0 +1	0 0 0	0 0 +1	+1
H L L L	H	17	H H H	L H H	0 0 0	−1 0 0	−1 0 0	−1
H L L H	L	18	H L H	L H H	0 +1 0	−1 0 0	−1 +1 0	0
H L L H	H	19	H L H	L H H	0 +1 0	−1 0 0	−1 +1 0	0
H L H L	L	20	L H L	H H H	+1 0 +1	0 0 0	+1 0 +1	+2
H L H L	H	21	H H H	L L H	0 0 0	−1 −1 0	−1 −1 0	−2
H L H H	L	22	L H H	H H H	+1 0 0	0 0 0	+1 0 0	+1
H L H H	H	23	H H H	H L H	0 0 0	0 −1 0	0 −1 0	−1
H H L L	L	24	H L L	H H H	0 +1 +1	0 0 0	0 +1 +1	+2
H H L L	H	25	H H H	L H L	0 0 0	−1 0 −1	−1 0 −1	−2
H H L H	L	26	H L H	H H H	0 +1 0	0 0 0	0 +1 0	+1
H H L H	H	27	H H H	H H L	0 0 0	0 0 −1	0 0 −1	−1
H H H L	L	28	L L L	H H H	+1 +1 +1	0 0 0	+1 +1 +1	+3
H H H L	H	29	H H H	L L L	0 0 0	−1 −1 −1	−1 −1 −1	−3
H H H H	L	30	L L H	H H H	+1 +1 0	0 0 0	+1 +1 0	+2
H H H H	H	31	H H H	H L L	0 0 0	0 −1 −1	0 −1 −1	−2

4.163 LOGICAL ERROR GENERATOR

4.164 Every time the ERROR TIMER line goes low, a logical error is generated. The logical error generator is comprised of U16A/B and U13C. Basically, the generator looks for the next available logical one in the T148 XMT DATA input and eliminates it. See Figure 4—14 for the timing diagram. The normal operating conditions before an error is requested is with U16B cleared and U16A preset. The high Q output of U16A enables the B IN half of SERIAL IN gate U5. The T148 XMT DATA normally passes to the shift register for further encoding. When errors are requested, a series of negative pulses approximately two-thirds of a second apart are present on the ERROR TIMER line. The rising edge of this pulse clocks U16B and its Q output goes high. The next logical one that appears on the #19 line forces the output of U13C low. The next time the T148 XMT CLOCK goes high, U16A is clocked and its Q output goes low. This inhibits the SERIAL IN gate of U5 and when the logical one detected on the #19 line appears on the T148 DATA line, it cannot be shifted into the register. This in effect causes a logical zero to be generated where there should have been a logical one. This will be detected as a logical error when the other end of the span line is monitored. The high-to-low transition of the U16A Q output also clears U16B to inhibit the error generation mode. Thus only one error is generated per negative pulse on the ERROR TIMER line.

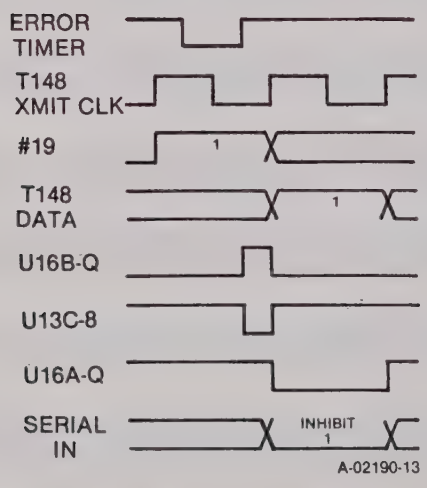

Figure 4—14. Logical Error Generator Timing Diagram

4.165 DISPARITY ERROR GENERATOR

4.166 Assuming that one Model 7040 is transmitting a T148 signal into a span line that is connected to a second Model 7040 at the other end, the disparity counter in both the transmitter and the receiver very quickly becomes synchronized. That is, the disparity counters at each end will track each other. To generate an error at the transmitter that will cause an error to be detected at the receiver requires that this synchronization be momentarily disrupted. This is the function of the disparity error generator comprised of U12A/B, U7A/B, and U9C all in conjunction with disparity counter U8.

4.167 See Figure 4—15 for the timing diagram. The beginning state when no errors are being requested is with U12A and U12B both cleared and U7A preset. U7B can be in either state depending on the polarity of the last disparity error that was transmitted. The low U12B Q output holds U12A cleared and it is unable to respond to its clock input supplied by U13B. The high U7A Q output, however, places U12B in a mode whereby it can respond to a clock pulse.

4.168 When errors are being requested, the ERROR TIMER line goes low for a short period approximately every two-thirds of a second. The rising edge of this pulse clocks U12B, which registers the error request. U12A is now free to respond to a clock pulse providing that the output of U9C is high and that the first bit of the next word supplied by U18 causes U8 to decrement. In terms of the disparity counter, this means that the QA through QD outputs are 1 0 0 0 respectively, which corresponds to a disparity of +1. With a positive disparity, the next word selected will have a negative disparity. The first bit of this word may or may not be a −1. If it is not, U12A will wait until both of the above stated conditions are present. At this time the output of U13B goes high and U12A is clocked. Its Q output goes low and the word present at the A through D inputs of U8 will be loaded into the counter. For discussion purposes, assume that the Q output of U7B is high. This means that 0001 will be loaded into U8. The 3-bit word presently being counted had to start with a −1 in order to get the error generator started. Therefore, the word must be −1 X −1, where x is either 0, −1, or +1. Thus depending on X, the word disparity can be either −1, −2, or −3. Since 1000 (+1 disparity) was loaded into the counter after it had already counted the first −1, the counter will always stop at a count that is one count more positive than it would have been. The next pulse on the ERROR TIMER line will clock U7B and the word loaded into the counter will be 0110 (−2 disparity). In this latter case, the counter will stop at a count that is one count too negative. The positive and negative disparity errors will alternate as long as errors are requested. See Table 4—9 for a table that describes the error disparity in terms of the word being counted and the loaded word.

Table 4—9. Disparity Error Versus Word Counted and Loaded

STARTING COUNT	NEXT WORD (*)	FINAL COUNT AFTER LOADING		FINAL COUNT IF NO ERRORS
		1000	0110	
1000	−1, +1, −1	1000 (+1)	0110 (−2)	0111 (−1)
1000	−1, 0, −1	0111 (−1)	0101 (−3)	0110 (−2)
1000	−1, −1, −1	0110 (−2)	0100 (−4)	0101 (−3)

*Positional variations would produce same word disparities.

4.169 QRSS RECEIVER ASSEMBLY A3 DETAILED CIRCUIT DESCRIPTION

4.170 See Figure 6—20 for the schematic diagram. The function of the QRSS receive assembly is to compare, bit-by-bit, the received QRSS data with a locally-generated QRSS signal and to generate a bit error every time they do not agree. The functional sections of the QRSS receive assembly include a standard QRSS generator, a 20-bit delay register, a logical error detector, and an error rate detector/synchronizer.

4.171 QRSS GENERATOR

4.172 The actual QRSS signal generator is made up of 20-bit shift register U6 through U8 and exclusive OR gates U16C/D. The Bell Standard quasi-random signal having a word length of 1,048,575 bits is created by returning bits 17 and 20 to the serial input of the shift register through exclusive OR gate U16D and gates U16C, U9A, and U9D. Normally, the output of U16D is applied to the B input of U8. The basic shift rate is controlled by CLK, which is a function of the system selected. The QRSS generator output is b. 20 (U6-QE).

4.173 QRSS specifications do not allow more tha... consecutive zeros in the transmitted bit stream. During normal operation, it is possible for the QRSS generator to produce up to 19 consecutive zeros. A 15 zero detector looks at the 15 bits preceding the output and when it detects all zeros, it stuffs logical ones into the output until the 15 zero condition no longer exists. The 15 zero detector consists of U11A-C, U12A-C, U13C, U17B, U20C, and U20A. When 15 zeros are detected, the output of U17B goes high, which is inverted by U20C. If T1C has not been selected, T1C SEL is low and the output of U20A is high. Since bit 20 is low at this time, the output of exclusive OR gate U16A will be high (logical one) as long as the 15 zero condition lasts. Fifteen zero suppression is not used when T1C is selected. During this time, T1C SEL is high and U20A is inhibited so that its output is held permanently low thus inhibiting the 15 zero detector.

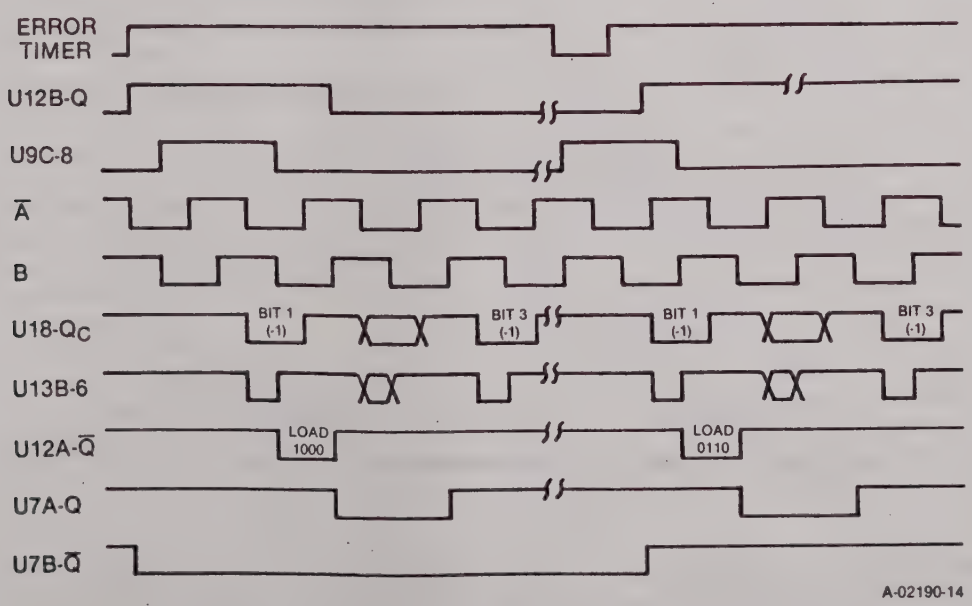

Figure 4—15. Disparity Error Generator Timing Diagram

4.174 When power is first applied to the unit, it is possible that the shift registers could have all low outputs. With no logical ones to shift into the serial input, all outputs would remain zeros permanently and normal operation would never begin. This condition is detected by a combination of the 15 zero detector previously described and an additional five zero detector comprised of U13A/B and U17A. If 20 zeros are detected, all of the inputs of U17A are high and its output goes high. This high level is passed by U16C to one input of U9A. Assuming that the received QRSS signal is synchronized to U8-2, the $\overline{Q}$ output of U14B is high and the output of U9A is low. At this time the output of U9D goes high forcing a logical one into the serial input of U8. This guarantees that 17 bits later a logical one will appear at bit 17, be fed back, and get normal QRSS operation started.

4.175 20-BIT DELAY REGISTER

4.176 Once the QRSS received data is synchronized with the serial input of U8, the received data must be delayed by 20 bits so that the QD output of U1 is still synchronized with the QE output of U6. Thus shift registers U1-U3 provide a simple 20-bit delay.

4.177 LOGICAL ERROR DETECTOR

4.178 The received QRSS signal and the locally-generated QRSS signal are compared bit-by-bit in exclusive OR gate U16B. The output of U16B will be low as long as its two inputs are identical. If they are not in agreement, the D input of U14A goes high. The next low-to-high CLK transition triggers U14A and its Q output goes high. The next time $\overline{CLK}$ goes high, the output of U9B goes low, which is inverted by U20B to provide a high bit error. The low output of U9B is also applied to the error rate detector/synchronizer.

4.179 ERROR RATE DETECTOR/SYNCHRONIZER

4.180 The function of the error rate detector/synchronizer is to detect a logical bit error rate in excess of 10^2, and to force resynchronization of the received and locally-generated QRSS signals. These circuits are comprised of U19, U18B, U4B, U11D, U18A, U14B, U9A/C, U5, U10, and U15. See Figure 4—16 for the timing diagram.

4.181 The error rate is monitored by looking at 1024-bit groups of the receive clock and counting the bit

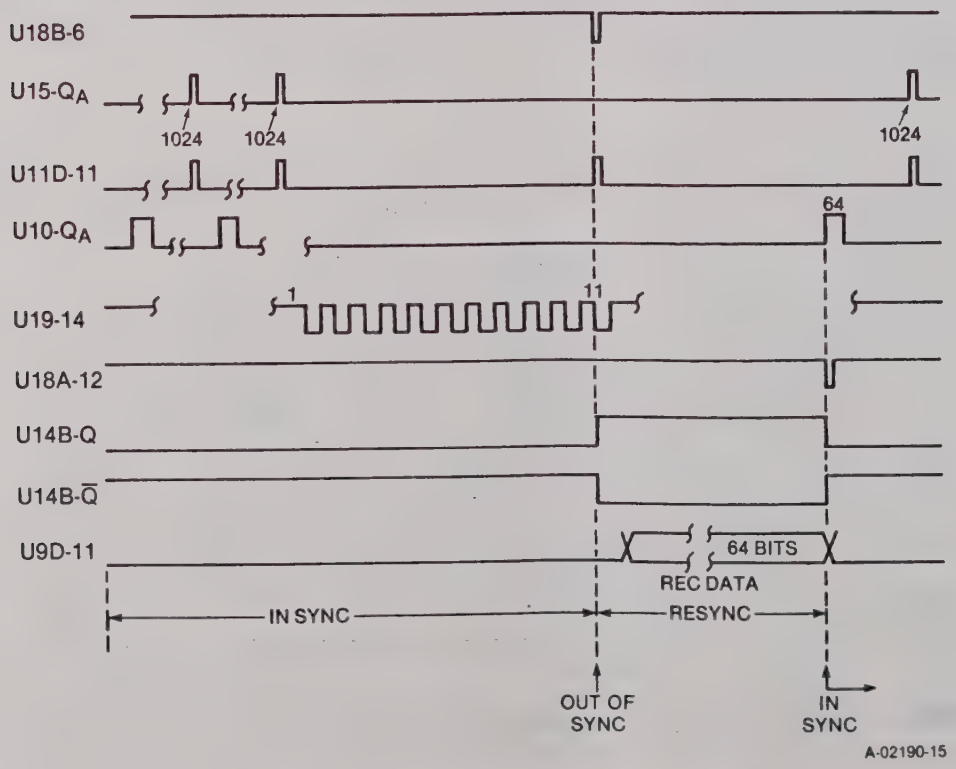

Figure 4—16. Error Rate Detector/Synchronizer

errors occurring during this period. The 1024-bit counter consists of U5, U10, and U15 while the error counter is U19 and U18B. Assuming that the two QRSS signals are in synchronization and the error rate is less than 10^2,U19 will register less than 11 counts during the time it takes to count 1024 clock pulses by U5, U10, and U15. Each time the count reaches 1024, the QA output of U15 goes high. This is passed by U11D to reset the 1024-bit and the error counters. During the in-sync condition, U14B is in the cleared state with its Q output low and its $\overline{Q}$ output high. This inhibits U9C and enables U9A. The serial input for the QRSS generator is the feedback supplied by bits 17 and 20 allowing the generator to free run.

4.182 When U19 reaches an error count of 11 during the 1024 pulse period, the error rate of 10^2 is exceeded and it is assumed that the two QRSS signals are not synchronized. At the count of 11, the U18B output goes low. This is inverted by U4B, passed by U11D, and resets both counters. As soon as U19 is reset, its outputs go low forcing the output of U18B high. This positive transition triggers U14B and its Q and $\overline{Q}$ outputs go high and low respectively. Gate U9A is inhibited while U9C is enabled. The received QRSS signal is now applied to both the 20-bit delay register and to the QRSS generator serial input. With its normal feedback path broken, the QRSS generator now acts as a simple 20-bit register. If at least 20 bits are shifted into both the 20-bit delay and the QRSS generator, they will be loaded with the same bit information and thus synchronized. Actually 64 bits are used to obtain synchronization in the following manner. During the 64-bit count, the QA output of U10 is low and U18A is inhibited. At the count of 64, this output goes high and the low output of U18A clears U14B. Feedback is returned to the QRSS generator and U18A is inhibited. This completes the resynchronization phase.

4.183 T148 RECEIVER ASSEMBLY A7 DETAILED CIRCUIT DESCRIPTION

4.184 See Figure 6—22 for the schematic diagram. The function of this assembly is to convert the received T148 ternary data to a binary form, provide a T148 receive clock that is synchronous with the output binary data, and to detect disparity errors.

4.185 TERNARY-TO-BINARY CONVERTER

4.186 The function of the ternary-to-binary converter is to convert 3-bit ternary data words into 4-bit binary words. See Figure 4—17 for the timing diagram. Inputs to the converter are the ± T148 PULSES, CLOCK(R) and 4Xϕ. These signals are synchronous with one another and in addition, the rising edge of CLOCK(R) is coincident with the middle of the pulse bit time. The + PULSES rail contains all pulses that were encoded as positive ternary pulses at the transmitter while the − PULSES rail contains the recovered negative pulses. The individual bits are at a 50 percent duty cycle. Assuming that the receiver is synchronized with the transmitter, the first bit of a word shifted into U3 by CLOCK(R) will in fact coincide with what was encoded as bit one of the same word at the transmitter. After three shifts, the 1Q through 6Q outputs of U3 represent a 6-bit address code. The five least-significant bits are used to select one of 16 8-bit words stored in PROM U4. The sixth and most-significant bit then selects one of two 4-bit words available at the input of multiplexer U10. Thus the 1Y through 4Y outputs of U10 represent the exact 4-bit binary word, in parallel format, that was encoded at the transmitter. Immediately after the third bit is shifted into U3, a negative load pulse locks the 4-bit words into output shift register U14. After a slight delay to allow the shift register outputs to settle, a series of four positive pulses supplied by U13B converts the parallel binary information into four serial binary bits. This completes the conversion and the cycle repeats.

4.187 SYNCHRONOUS CLOCK GENERATOR

4.188 The function of the synchronous clock generator is to create a T148 REC CLOCK output that is synchronous with the T148 REC DATA output. The generator consists of U11A, U9, U12B, U8C and U13A/B. Assuming that synchronization has been attained, the level at U12D-13 will be a steady high. A convenient starting point is to assume that U13A-Q has just gone low to clear U11A. This forces its Q output low, clearing counter U9 and U13B. On the rising edge of the next CLOCK(R) pulse, U11 is triggered and its Q output goes high freeing U9 and U13B. With both the QA and QD outputs of U9 low after being cleared, the output of U12B goes high. The next positive transition of 4Xϕ triggers U13B. Its Q output goes high to start the first received clock pulse and its Q goes low creating the first shift pulse used by the output shift register. Counter U9 proceeds to count 4Xϕ pulses and its QA output is applied through U12B to the D input of U13B. The T148 REC CLOCK is generated when U13B toggles to follow its D input. The clock consists of four positive pulses followed by a dead period. It is synchronous with the T148 REC DATA output. When U9 has counted eight 4Xϕ pulses, QD goes high. This, along with the high Q output of U13A, forces the output of U8C low. On the next rising edge of 4Xϕ, U13A is triggered and its Q output goes low. This is the load pulse for U14 and the clear pulse for U11A and completes the clock cycle, which then repeats after a dead period.

4.189 Up until now it has been assumed that the three bits shifted into U3 were in fact the same three bits of words as transmitted. At power up or as the result of any

signal interruption, synchronization will probably be lost. Regaining synchronization is the function of U7B/C, U2B, and U12A, C, and D along with the clock generator already described. The timing diagram shown on Figure 4—18 represents a one-bit out-of-sync condition. The three bits shifted into U3 are parts of adjacent ternary words as they were transmitted. During the in-sync condition of normal operation, all three bits of any ternary-encoded word cannot be logical zeros. This is the result of the encoding scheme used. When synchronization is lost, however, three consecutive logical zeros that are parts of adjacent words will very quickly be shifted into U3. Both rails of the T148 ± PULSES input will be zeros so that after the third shift, all six Q outputs of U3 will be low. These are decoded by U7B/C and the output of U2B goes low. At the end of the next four-bit clock cycle, the Q output of U13A goes low forcing the output of U12A high. Gates U12C/D are cross-connected to form an R-S flip flop. The high U12A output sets the flip flop and the D input of U11A goes low. Since the U11A Q output has just been cleared low, the rising edge of the next CLOCK(R) pulse has no effect on U11A. This has the overall effect of delaying the start of the next four-bit clock cycle until the next CLOCK(R) pulse.

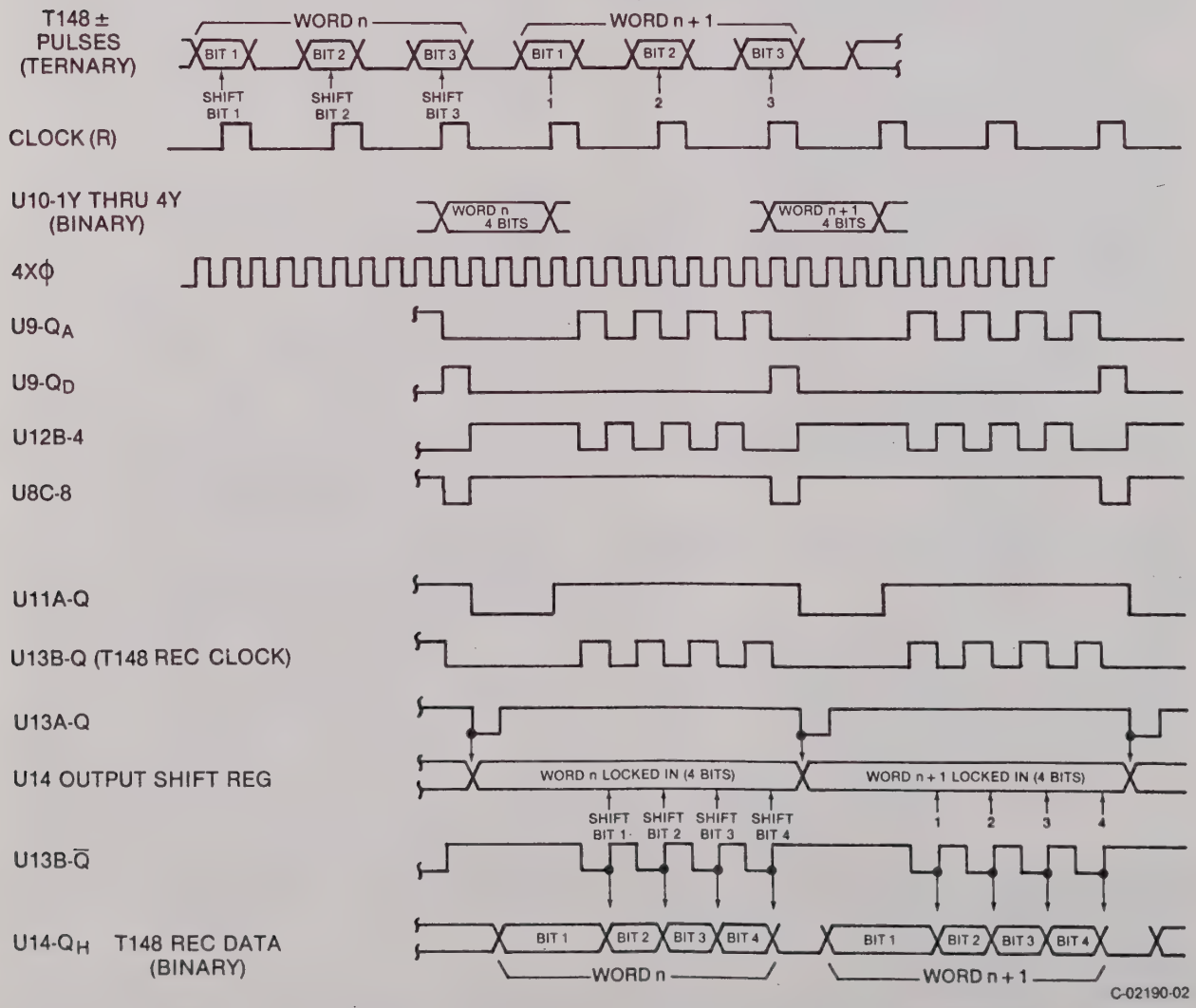

Figure 4—17. T148 Receiver 3 Ternery-To- 4 Binary Converter Timing Diagram.

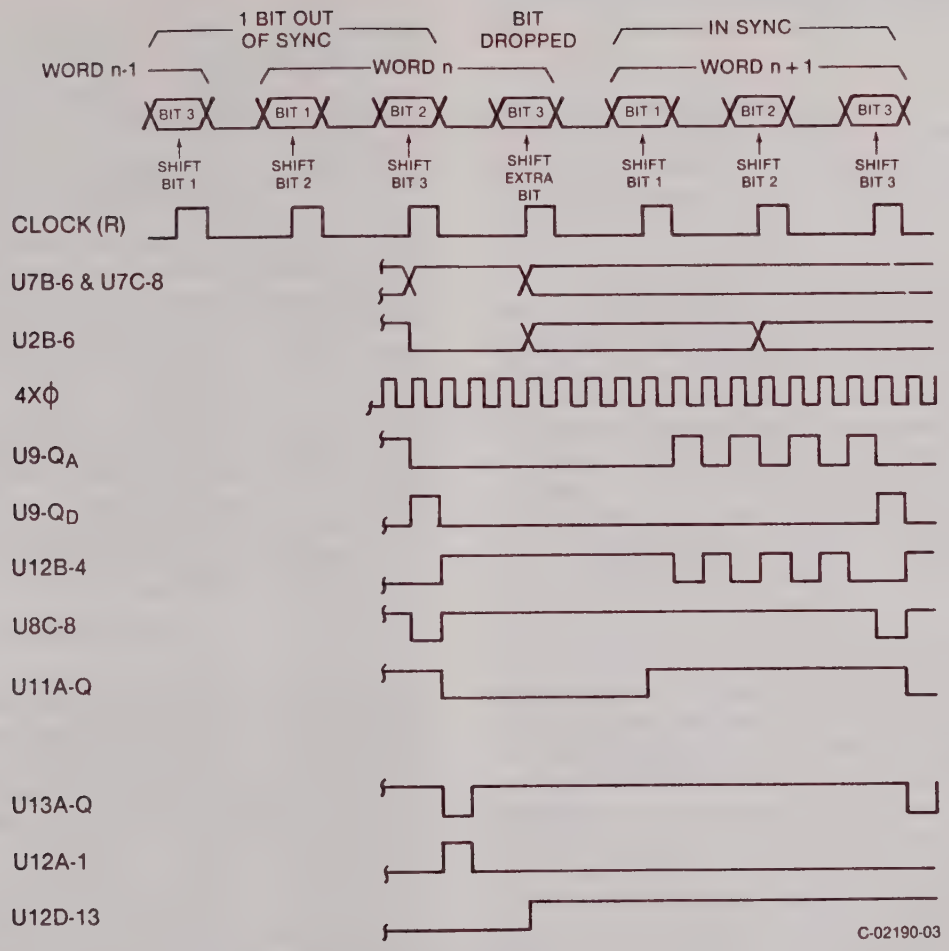

Figure 4—18. T148 Receiver 3 Ternery-To-4 Binary Converter Bit Synchronization Timing Diagram.

4.190 A bit is shifted into U3 every time there is a rising edge of CLOCK (R). Normally three bits are shifted in and then locked into U14 by the load pulse at the end of the clock cycle. Since the clock cycle has been delayed one whole CLOCK (R) cycle, four bits will be shifted into U3 before the next load pulse locks data into U14. As shown on the timing diagram, the first bit shifted is bit three of one word and the last three are the complete next word. Since U3 can only hold three bits of each rail, the first bit shifted in gets overwritten and is lost. The three remaining bits are the ones desired. At the end of the next clock cycle these bits will be locked into U14 and synchronization will be re-established.

4.191 DISPARITY ERROR DETECTOR

4.192 The function of the disparity error detector is to generate a pulse each time the disparity exceeds its allowable limits. The detector is comprised of U8A/B, U6, U1A-D, U5C, and U2A/C. Table 4—10 shows that after start up, disparity is not allowed to exceed +4 or −4. Disparity is the long-term difference between positive ones and negative ones. This difference can be kept track of very conveniently by using an up-down counter. As long as the disparity remains within the range of −3 to +3 inclusive, the outputs of U5A/B will both be high. These enable one input each ofU8A/B. When CLOCK(R) is high, positive ones will increment U6 through U8A and negative ones will decrement the counter through U8B. When disparity reaches the +4 limit, the QA-QC outputs of U6 force the output of U5A high. If the next bit received is a negative one, it will pass through U8B, decrement the counter, and operation continues by returning the output of U5A high. However if the next bit is a positive one, the low output of U5A inhibits U8A and the count remains at a +4 disparity. In addition, the output of U5C goes low to generate a positive disparity error pulse at the output of U2A. An exact operation occurs when the disparity reaches −4.

4.193 INTERFACE ASSEMBLY A4 DETAILED CIRCUIT DESCRIPTION

4.194 See Figure 6—24 for the schematic diagram. The function of the interface assembly is to detect bipolar violations, oscillations, provide an interface for the front panel LED indicators, and to multiplex errors, clocks, and data for use throughout the unit.

4.195 BIPOLAR VIOLATION DETECTOR

4.196 The function of the bipolar violation detector is to examine the T1 and T1C recovered data bit streams for violations of the normal alternate-mark-inversion format. These violations are usually the result of pulse additions or deletions when passing through line repeaters. When no violations are present, logical ones alternate between the +PULSES line and the −PULSES LINE. The third input to the detector is the DATA line, which is the summation of the ±PULSES lines. The detector consists of U3A, U7D, and U7A/B.

4.197 As shown on Figure 4—19, the normal alternating logical ones appearing at the J and K inputs of U3A cause the flip flop to toggle on the falling edge of its clock input. Thus when there are no bipolar violations present, positive pulse coincidence can never occur at either U7A or U7D. When two consecutive pulses appear on the +PULSES line, U3A does not toggle on the second pulse. The Q output of U3A remains high and the presence of the second positive pulse causes the output of U7D to go low. This is inverted by U7B to create a positive bipolar violation error pulse. The same situation occurs when two consecutive pulses appear on the −PULSES line.

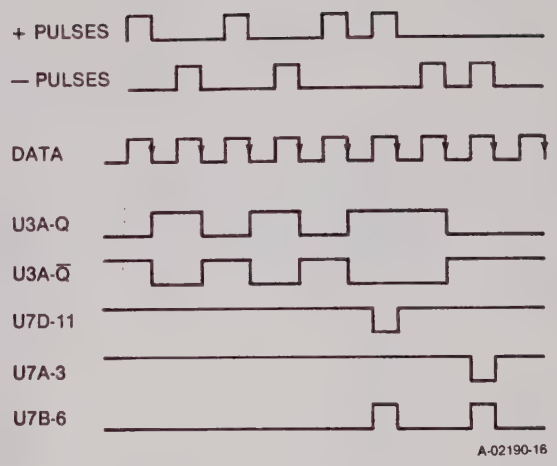

Figure 4—19. Bipolar Violation Detector Timing Diagram

4.198 OSCILLATION DETECTORS

4.199 The function of the two oscillation detectors is to detect the presence of frequencies below 20 kHz in one case and an all ones signal above 774 kHz in the other. The low frequency detector is comprised of U2B, U6A, U6B, and U2D while the high frequency one consists of U2A, U6C, U6D, U9C, and U5A.

4.200 The low frequency oscillation detector is made up of two integrator/comparators. The input stage is a long pulse detector with the integrator time constant of 46.4 microseconds set by R11 and C5. The following

Table 4—10. Disparity Counter U6 Truth Table

DECIMAL COUNT	DISPARITY	OUTPUTS Q_D	Q_C	Q_B	Q_A	
4	+5	L	H	L	L	NOT ALLOWED AFTER START-UP
3	+4	L	L	H	H	8 ALLOWABLE OPERATING STATES
2	+3	L	L	H	L	
1	+2	L	L	L	H	
0	+1	L	L	L	L	
9	−1	H	L	L	H	
8	−2	H	L	L	L	
7	−3	L	H	H	H	
6	−4	L	H	H	L	
5	−5	L	H	L	H	NOT ALLOWED AFTER START-UP

stage is a minimum time duration detector. The integrator time constant of 2.61 milliseconds is set by R9 and C4. Each integrator is connected to the negative input of a voltage comparator. The positive comparator input is a reference voltage of +3.2 volts determined by R15 and R16. Since +3.2 volts represents 63 percent of the available supply voltage, the integrators will charge to this voltage in one time constant. Frequency is determined indirectly by observing the time between pulses, which is inversely proportional to frequency. The presence of pulses at the input of U2B is represented by a high level and the time between them is low. These are inverted by U2B and then applied to the long pulse detector. When the frequency is less than 20 kHz, the high time between pulses is greater than 46.4 microseconds and C5 charges to at least +3.2 volts. Since its reference voltage has been exceeded, comparator U6A discharges C4. This reduces the voltage at the negative input of U6B below +3.2 volts and the comparator is turned off. The input of U2D is pulled high through R10 and the low output of U2D is applied to the interface circuit via U1C.

4.201 If the input frequency is greater than 20 kHz, the time between pulses is not long enough to allow C5 to charge to the reference voltage. This turns off comparator U6A allowing C4 to start charging. If the high frequency is present for at least 2.61 milliseconds, the voltage on C4 will exceed the reference voltage. Now the output of U6B goes low. This is inverted by U2D and the high level is blocked by U1C.

4.202 The all ones oscillation detector makes the distinction between an all ones signal and a normal T1 signal as long as the frequency is greater than 774 kHz. This detector is identical in operation to the low frequency one just described. The long pulse integrator time constant is 1.1 microseconds set by R6 and C2 while the minimum time integrator time constant is 10 milliseconds set by R7 and C3. In a normal T1 signal, random logical zeros in the bit stream appear often enough to make it distinguishable from an all ones signal. Every time a zero is present, C2 charges to a level greater than the reference voltage and the output of comparator U6C goes low. This discharges C3 of whatever voltage it had attained during the period between zeros. This occurs often enough so that the voltage on C3 never exceeds the reference voltage and the output of comparator U6D remains high. This is blocked by U9C.

4.203 When the input is greater than 774 kHz and is all ones, C2 never charges to a voltage greater than the reference voltage. This turns off comparator U6C and C3 starts to charge. If the all ones condition lasts for 10 milliseconds or longer, C3 charges to a level that exceeds the reference voltage and the output of comparator U6D goes low. If the T1 system has been selected, the $\overline{\text{T1 SEL}}$ line will be low. The high output of U9C is inverted by U5A and applied to the interface circuit via U1C.

4.204 INDICATOR INTERFACE

4.205 The function of the indicator interface is to decode the pulses, errors, and oscillations detector ouputs and set the on time duty cycle for the front panel LED indicators.

4.206 The ERRORS LED indicator interface circuit is comprised of U2E, U8A-C, U12A/B, U5B, and U9B. If the LOGICAL (QRSS) errors function has been selected, the LOGIC ERROR SELECT line will be pulled up through R1. This enables one input of U8A and the inverted low inhibits U8B. Positive pulses appear on the LOGICAL BIT ERRORS Line each time a logical error is detected. These pulses are passed by U8A and U8C and appear at the B input of 50-millisecond one shot U12B. The first falling edge triggers U12B and its Q and $\overline{\text{Q}}$ outputs go high and low respectively. The low $\overline{\text{Q}}$ output triggers U12A, which applies a high level to the A input of U12B. This prevents retriggering for 110 milliseconds. Thus U12B can be triggered every 100 milliseconds and its Q output remains high for 50 milliseconds of this time. This represents an on time duty cycle of approximately 50 percent. The one shot output is applied to U9B and lights the ERRORS LED located on the front panel.

4.207 When the violations function has been selected, the LOGIC ERROR SELECT line is low. This inhibits U8A and the inverted high level enables one input of U8B. Either bipolar violations or disparity errors are present at the 4Y output of multiplexer U4. They are passed by U8B and U8C and trigger the one shot exactly as described for logical errors. The output of U8C is buffered by U5B and made available at the ERROR DET OUT jack. When low frequency oscillations are being detected, U8C is inhibited. The massive errors present during this condition are thus prevented from reaching the ERRORS indicator.

4.208 The second interface circuit functions as a decoder to light the appropriate combination of the PULSES and OSC indicators for displaying the presence of pulses, low frequency oscillations, and all ones oscillations. The circuit is comprised of U11A/B, U1B, U7C, U5D/F, and U9A/D.

4.209 When normal data is being received but there are no oscillations, the output of U1C is low and U7C is inhibited. One shot U11A is triggered by the data pulses and a 50 percent duty cycle high output is applied to one input of U1B. The second input is also high and the PULSES indicator is lighted through U5F and U9A. For low frequency oscillations, U1B is inhibited and U7C enabled. The output of U11A is used to light the OSC

indicator through U5D and U9D. For all ones oscillations, both U1B and U7C are enabled. In this case, both the PULSES and the OSC indicators are lighted.

4.210 When the power switch is held in the LAMP TEST position, one input to U9A, U9B, and U9D goes high. This is applied to all of the LED indicators for a test. In addition, the low output of U5C inhibits triggering of U12B and U11A so the test can be made.

4.211 MULTIPLEXER

4.212 The function of the multiplexer is to select either the T148 or T1/T1C data and clocks for use by the QRSS transmitter and the QRSS receiver. The circuit consists of U4, U1A/D, and U2F.

4.213 When T148 and either current, voltage, QRSS, or transmit errors have been selected, the output of U1A goes low. This enables the T148 transmitter and also is inverted by U2F to select the B inputs of U4 and apply them to the Y outputs. All of the B inputs are associated with the T148 system. These outputs are then applied to the QRSS receiver and transmitter. When either T1 or T1C is selected, the low T148 SEL line inhibits U1A. Its high output is inverted by U2F and selects the A inputs to U4. All of these inputs are associated with T1 or T1C.

4.214 ARTLINE ASSEMBLY A11 DETAILED CIRCUIT DESCRIPTION

4.215 See Figure 6–26 for the schematic diagram. The function of the artline assembly is to generate a sine wave interfering signal at a frequency one half the T1, T1C, and T148 bit rates, sum this signal with a normal PCM signal, and simulate the loss and frequency response of various lengths of cable. The assembly is comprised of two functional sections; the Near End Cross Talk (NEXT) generator and the artificial line.

4.216 NEXT GENERATOR

4.217 The function of the NEXT generator is to generate a sine wave interfering signal at either 770 kHz, 1.15 MHz, or 1.54 MHz and to provide selected output levels referenced to a full strength all ones signal as it would appear at a repeater input.

4.218 Crystal Y1 and transistor Q5 form a 9.238 MHz oscillator that generates a distorted sine wave output. The signal is squared up by Q7 and the falling edge is used to trigger counters U6 and U7. The combination of U7 and U8 results in a 770 kHz output at QC. The QB output is at 1.54 MHz while the output of U6 is at 1.15 MHz. SYSTEM switch S1 applies a selected ground to either U9B, U9C, or U9A. The grounded gate is enabled and passes the associated signal to a band pass filter that removes all of the associated harmonics from the square wave and leaves the sine wave fundamental. Calibration potentiometers R78, R79, and R80 are used to adjust the signal level for 0 dBm at the input to the output emitter follower. The selected sine wave is applied to output emitter follower Q6 that matches the low impedance of the attenuator string and the output transformer. INTERFERENCE MARGIN (dB) switch S2 selects one of 11 attenution factors in one dB steps and applies the attenuated signal to output transformer T2. The attenuation factors represent a signal level below that of an all ones signal that would normally be present at the input of a repeater.

4.219 ARTLINE

4.220 The function of the artline is to sum the interfering signal and the normal PCM signal generated on another assembly. Linear summing takes place in resistors R2 and R3 before being applied to the artificial line. The artline consists of five active stages that have three-pole feedback networks. The first four stages are identical and have a loss of 9 dB at 772 kHz. The final stage has six separate feedback networks with losses of 0, 2, 4, 5, 6, and 7 dB at 772 kHz. The five decks of LINE LOSS (dB) switch S3 select combinations of feedback networks that total the losses indicated on the switch. In addition to providing the indicated losses at the center frequency of the T1 bit rate, the artline provides a frequency response designed to match that of an average response obtained from PIC and pulp cables.

4.221 The output stage of Q2 and Q4 is a complementary emitter follower configuration. This provides the drive capability needed for the 200 ohm load offered by R63 and T1. Bias for the output stage is provided by R57, Q1, Q3, and R58. Transistors Q1 and Q3 are connected as diodes and provide a measure of stability for temperature variations.

4.222 ANALOG FAULT LOCATE ASSEMBLY A10 DETAILED CIRCUIT DESCRIPTION

4.223 See Figure 6–28 for the schematic diagram. The function of the assembly is to normalize each of the 10 full scale fault locate input ranges to a constant level and dynamic range, compensate for differences in the level of the fault locate return signal due to pulse periods, provide a C-message noise filter, present an extremely narrow band pass to the fault locate signal, and provide a meter reading that is approximately proportional to the rms level of the fault locate signal.

4.224 INPUT SIGNAL NORMALIZER

4.225 The function of the input signal normalizer is to convert all full scale fault locate signal ranges to a

constant level of −60 dBm at the input of U3. This is accomplished through the use of various combinations of attenuation and amplification. The first step in normalization consists of compressing the 90 dB input dynamic range to two sub ranges, each having a 40 dB dynamic range. This is accomplished with a 40 dB attenuator comprised of R56, R57, and R58 and the switching of RECEIVE LEVEL dBm/dBrn switch S1A. After 10 dB of amplification provided by U1, the two 40 dB dynamic ranges at the output of U1 range from −30 to −70 dBm to −40 to −80 dBm. These correspond to the input ranges of −90 to 0 dBm respectively. Neglecting for a moment the 60 Hz reject and C-message filters, the final step in normalizing the input ranges to a constant level is provided by U2 and a six-level step attenuator. As a result of the levels present at the input of U2, the 20 dB of amplification provided by U2, and the attenuation factors of the step attenuator selected by S1B, the level across R91 is a constant −60 dBm at full scale for all ranges of the fault locate signal.

4.226 60 HZ REJECT AND C-MESSAGE FILTERS

4.227 To minimize the effects of induced 60 Hz power line voltage, a reject filter comprised of C42, L3, C41, and R96 is used. The loss at 60 Hz is at least 50 dB. When FAULT LINE LEVEL/NOISE switch S3 is set to LEVEL the output of the reject filter is applied to U2 through the normally closed contacts of K2.

4.228 When measuring noise on the fault line, the C-message filter provides the standard Bell noise response. An input amplifier consisting of Q10 and Q7 compensates for the mid-band loss at 1 kHz. The active high pass portion of the bandpass filter is made up of Q8, Q9, C18, C19, R48, and R38. This is followed by emitter follower Q6. The low pass part of the filter is comprised of R33, R29, C15, and C16. The output emitter follower stage is Q4. When S3 is set to NOISE, K2 is operated and the output of the C-message filter is applied to U2.

4.229 PULSE PERIOD GAIN COMPENSATION

4.230 As the fault locating signal pulse period is cycled from 11 to 4, the level of the audio component returned to the unit increases due to the increasing pulse density. Compensation is accomplished by changing the gain of U3 in synchronization with the change in pulse period. Analog input switch U5 is in effect a series of single-pole, single-throw switches controlled by the BCD count of the PPA, PPB, and PPC inputs. At pulse period 11, all three inputs are low and R85 is connected in the feedback path of U3. Thus the reference gain is set at +35 dB. As the pulse period is stepped down toward 4, different resistors are selected and the gain gradually drops to +24.9 dB at pulse period 4. An additional gain of +20 dB is provided by U4A/B, connected in a unity gain push pull arrangement. This gain includes the contribution of T1 so that the final normalized level at the secondary of T1 is −5 dBm at full scale fault locate input levels.

4.231 DIGITAL BANDPASS FILTER

4.232 To increase the accuracy of the fault locate measurement, an extremely narrow bandpass digital filter is used. This has the effect of greatly increasing the signal-to-noise ratio. A bandpass of approximately 1 Hz at the fault locate audio frequencies is realized by use of a digital, eight-section RC, commutative filter. The values of R89 and C22 through C29 determine the bandwidth of the filter while the center frequency is a function of the commutating (switching) rate determined by FLA, FLB, and FLC. Thus a fixed bandwidth for all center frequencies is obtained and the center frequency is changed simply by changing the commutative frequency in synchronization with changes in the fault locate frequency. FLA-FLC and the fault locating frequencies are derived from the same source and FLC is exactly the same frequency as the fault locating signal.

4.233 As shown on Figure 4−20, FLA-FLC generate eight timing intervals per cycle of fault locate signal. These are used to sequentially activate, what is in effect, eight single-pole, single-throw switches contained in U6. These switches sequentially ground capacitors C22 through C29. While each capacitor is grounded, the voltage across it represents the average voltage of the input signal during that interval. Capacitors not selected have no effect on the output. Thus the signal at the positive input of U10A is a staircase waveform replica of the sinewave input. In the example on Figure 4−20 the fault locate signal is shown synchronous and in phase with FLC for simplicity.

4.234 Since the staircase waveform output of the digital filter contains many harmonics as well as the desired fundamental fault locating frequency, these harmonics must be removed. This is the function of U10A, C52, C51, U10B, C54, C55, U10C, and the resistors selected by the multiple decks of LINE FILTER switch S2. Together they form an active lowpass filter. When measuring level, K1 is not operated and the fault locate signal is applied to U7A through the normally closed contacts of the relay. During noise measurement, however, K1 is operated and the digital filter is bypassed.

4.235 QRMS DETECTOR AND METER DRIVER

4.236 The function of the QRMS detector is to generate a dc voltage proportional to the quasi rms value of the fault locate signal input. Voltage follower

U7A provides isolation between the digital filter and the detector. Taken together, U8A and U8B form a full wave rectifier. At the output of U8A, the positive half cycles are applied through CR2 to the inverting input of U8B and appear as negative half cycles at the input of U9. The negative half cycles are applied through CR3 to the non-inverting input of U8B. Similarly they are negative going at the input of U9. The diodes in U9 cause the dc voltage from the rectifier to be proportional to the rms value of the sinewave signal being measured. The ripple component is removed by lowpass filter C6. The meter is placed in the negative feedback loop of driver U7B. Potentiometers R19 and R11 are used to calibrate the measurement circuits.

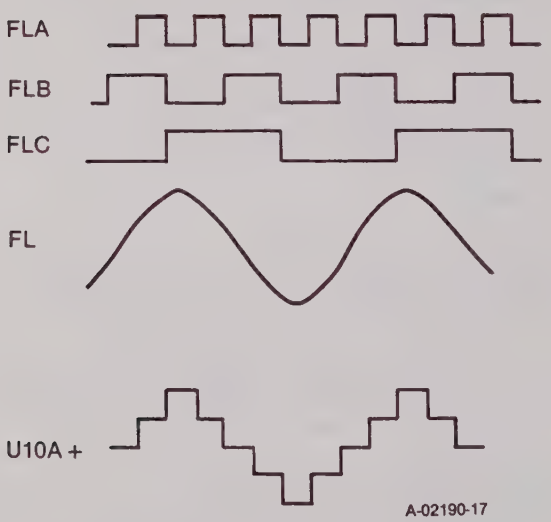

Figure 4—20. Digital Filter Timing Diagram.

4.237 REPEATER TEST ASSEMBLY A13 DETAILED CIRCUIT DESCRIPTION

4.238 See Figure 6—30 for the schematic diagram. The function of the assembly is to provide an interface between a span line or repeater under test and the transmitter and receiver functions in the unit. The three functional sections are the receiver interface, the transmitter interface, and the repeater test. The repeater test functional section has been previously described in paragraphs 4.90 through 4.96.

4.239 RECEIVER INTERFACE

4.240 The function of the receiver interface circuit is to convert the balanced PCM input, from either a span line or a repeater under test, to a pair of single rail pulse outputs as well as a double rail output. These are used throughout the receive and clock recovery functions. The PCM T and R input is applied to T1 through current limiters R20 and R21. Diodes CR12 through CR16 provide transient voltage protection. The out-of-phase signals at pins 16 and 13 of T1 are both referenced to ground and are applied to voltage comparators U4 and U5. In addition, the waveform at T1-16 is applied to variable threshold circuit U3. Resistors R23 and R22 attenuate the signal 50 percent and the amplitude of the signal present at the non-inverting input of U3 is always exactly one half of the received signal. Since U3 is connected as a voltage follower, the voltage at the junction of CR19 and C23 must also be equal to the peak positive voltage at the non-inverting input. This voltage is derived from a peak detector formed by CR19 and C23. The time constant of C23-R42 is very long in relation to the input pulse duration and thus the voltage across C23 represents the long-term average of one half the peak amplitude of the received input. This reference voltage is applied to one input each of comparators U4 and U5. Whenever the received pulse amplitude exceeds this reference, the output of the associated comparator goes low.

4.241 When there is no input signal, the voltage across C23 would normally decrease to zero. This would result in an unstable condition at the comparators and their outputs would be unpredictable. As the result of circuits further down stream, some of the front panel indicators would flash. To prevent this condition, U6 furnishes a +50 millivolt output when there is no input. Normally CR20 is reverse biased by the voltage across C23. When this voltage drops below 50 millivolts, U6 provides a +50 millivolt reference, which is applied to C23 through CR20. This forces the output of both U4 and U5 high and remains stable for a no signal condition.

4.242 The low comparator outputs are inverted by U2A/B to form the double rail outputs designated +PULSES and −PULSES. Both rails are made up of positive-going pulses and the terms positive and negative refer either to the pulse polarity of a normal bipolar bit stream or to the pulses defined by T148 encoding. In reference to the signal input at T1, a pulse on the +PULSES rail was a positive-going pulse on the tip and a pulse on the −PULSES rail a positive-going pulse on the ring. The double rail pulses are summed in NOR gate U2C and inverted by U2D to form the unirail outputs designated $\overline{\text{DATA}}$ and DATA respectively.

4.243 TRANSMITTER INTERFACE

4.244 The function of the transmitter interface circuit is to convert any of the transmit signals presented in a double rail format to a balanced tip and ring full strength output at the GENERATOR jacks. Inputs from the transmit circuits are designated T DATA and R DATA.

All logical ones appearing at these inputs are negative-going. In respect to the T148 system, + ones are present at the T DATA input and − ones at the R DATA input. For T1 and T1C systems, alternate ones appear at the two rails. During all transmit modes, $\overline{\text{STOP XMT}}$ is high and both U1A and U1B are enabled. Thus a logical one is represented by a high level at the base of Q2 or Q3. Both will never be high simultaneously.

4.245 When Q2 is turned on, its collector voltage drops and the voltage at the junction of R10 and R11 rises. Q4 is turned on and connects +6 volts to T2-3. At the same time, Q7 is turned on to connect ground to T2-6. Similarly, when Q3 is turned on +6 volts is applied to T2-6 and ground to T2-3. At the secondary of T2, the balanced output has a signal level of 6 volts peak-to-peak. Diodes CR5 through CR9 provide transient voltage protection. The PCM signal is then sent to the GENERATOR jacks located on the front panel.

4.246 The output peak-to-peak amplitude is calibrated by R5, which controls the dc voltage furnished Q4 and Q6. The +15 volt supply input is dropped down to +6 volts by emitter follower type voltage regulator Q1.

4.247 POWER SUPPLY ASSEMBLY A14 DETAILED CIRCUIT DESCRIPTION

4.248 See Figure 6−32 for the schematic diagram. The function of the assembly is to generate all of the operating voltages for the unit in general and to provide a variable constant current supply for the repeater under test in the unit.

4.249 The −200 volts used to check the insulation resistance of a repeater under test is provided by half wave rectifier CR20. Lowpass filtering is provided by R6 and C14.

4.250 When testing an office repeater, it is powered from an unregulated −55 volt source. This voltage is provided by full wave bridge rectifier CR11-CR14. Filtering is provided by C10.

4.251 The general operating voltages of +5 volts, +15 volts, and +15 volts are all regulated sources. Full wave bridge rectifier CR1-CR4 and A14U1 provide the regulated +5 volt output. The ±15 volt outputs are derived from bridge rectifier CR5-CR8 and regulated by A14U2 and A14U3.

4.252 A line repeater under test requires a constant current supply within the range of 50 to 200 milliamperes. This is the function of variable constant current source U1, U2, A14Q1, and Q1. Bridge rectifier CR15-CR18 furnishes a raw supply of approximately −37 volts. This is the input to the current regulator and is also used when testing an office repeater. Five volt regulator U1 supplies a stable reference voltage against which to compare the voltage drop across R9 caused by any change in the load current. Any change in the current output is sensed by R9 and unbalances the inputs of U2 in such a manner as to alter the output current in the opposite direction. CURRENT ADJ A12R1 allows the regulated current to be set within the range of 50 to 200 milliamperes.

SECTION 5

CALIBRATION

5.1 INTRODUCTION

5.2 This section provides a list of test equipment and individual calibration procedures required to calibrate the Model 7040.

5.3 TEST EQUIPMENT REQUIRED

5.4 Table 5—1 is a list of the test equipment required for calibration along with the critical specifications so that alternate pieces of test equipment can be selected.

Table 5—1. Test Equipment Required For Calibration

EQUIPMENT TYPE	TYPICAL MODEL (OR EQUIVALENT)	CRITICAL SPECIFICATIONS
Ac Voltage Calibrator	Fluke 5200A	Level Accuracy: ± 0.05 dB Phase Lock: must be able to phase lock on external signal
Frequency Counter	Ballentine 5500B	Accuracy: ± 5 counts No. Digits: 7 min.
Oscilloscope	Tektronix 465	Bandwidth: 100 MHz Inputs: Dual Channel
Probes (2 required)	Tektronix	Type: X10 Cable Length: 1 meter Frequency Response: 100 MHz
H Attenuator	—	Accuracy: ± 0.05 dB Impedance: 600 ohms
Ac Voltmeter	Hewlett Packard 400 FL	Frequency Response: 100 MHz; dB scale: Calibrated for 600 ohms
IC Test Clip	—	Type: 16 Pin DIP
Load Resistor	—	Resistance: 100 ohms ± 1%
Buildout Resistor	—	Resistance: 600 ohms ± 1%

5.5 CALIBRATION PROCEDURES

5.6 The following paragraphs provide step-by-step calibration procedures for the unit. Each major procedure is entirely independent of all others although the step-by-step procedures themselves must be followed in the order presented.

5.7 CLOCK FREQUENCY ADJUSTMENTS

5.8 This procedure is used to adjust the frequency of the basic oscillators that provide the T1, T1C, T148, and the fault locate outputs. To adjust the frequencies, perform the following steps.

1. Remove the four front panel screws and the four rear panel screws and slide the cover off to the rear.

2. Remove clock assembly A5, insert the card extender in the slot, and plug A5 into the extender. See Figure 5—1.

3. On the interconnection board located on the underside of the unit, connect the frequency counter input to J5-D. See Figure 5—2. Connect the frequency counter ground to the 7040 chassis ground.

4. Plug the 7040 power cord into an ac outlet.

5. Set the 7040 POWER switch to ON.

6. Set the 7040 SYSTEM switch to T1.

7. On A5, adjust C5 to obtain a frequency counter indication of 6,176,000 Hz. See Figure 5—3.

8. Set the 7040 SYSTEM switch to T1C.

9. On A5, adjust C7 to obtain a frequency counter indication of 12,608,000 Hz. See Figure 5—3.

10. Set the 7040 SYSTEM switch to T148.

11. On A5, adjust C6 to obtain a frequency counter indication of 9,480,000 Hz. See Figure 5—3.

12. Move the frequency counter input lead to J5-N. See Figure 5—2.

13. On A5, adjust C27 to obtain a frequency counter indication of 1,544,505 Hz. See Figure 5—3.

14. Set the 7040 POWER switch to OFF.

15. Remove the frequency counter.

16. Remove A5 from the extender and plug the assembly into the slot.

17. Slide the cover on and replace the eight screws.

5.9 GENERATOR OUTPUT LEVEL ADJUSTMENT

5.10 This procedure is used to set the peak amplitude of the signal at the GENERATOR OUT jack. To adjust the output level, perform the following steps.

1. Remove the four front panel screws and the four rear panel screws and slide the cover off to the rear.

2. Wire a 100 ohm, 1% resistor across the tip and ring of a 310 plug.

3. Insert the plug and resistor combination into the GENERATOR OUT jack.

4. Connect one of the X10 oscilloscope probes to one side of the 100 ohm resistor and a second X10 probe to the other side of the resistor. Connect the ground lead on each probe to the 7040 chassis ground.

5. Whatever control combination is required on the particular oscilloscope being used, it is important that the signal be displayed in the differential mode. On a typical oscilloscope this would be accomplished by selecting both channels and inverting one of them. Use the same vertical amplifier sensitivity for both channels.

6. Plug the 7040 power cord into an ac outlet.

7. Set the 7040 controls as follows:
   Function switch to QRSS
   SYSTEM switch to T1
   POWER switch to ON

8. As shown on Figure 5—4, the positive peak amplitude should be within the range of 2.7 to 3.3 volts measured base-to-peak. If it is not, adjust R5 on A13 to obtain an oscilloscope indication of 3.0 volts base-to-peak. See Figure 5—2.

9. Remove the oscilloscope and the plug/resistor combination.

10. Set the 7040 POWER switch to OFF.

11. Slide the cover on and replace the eight screws.

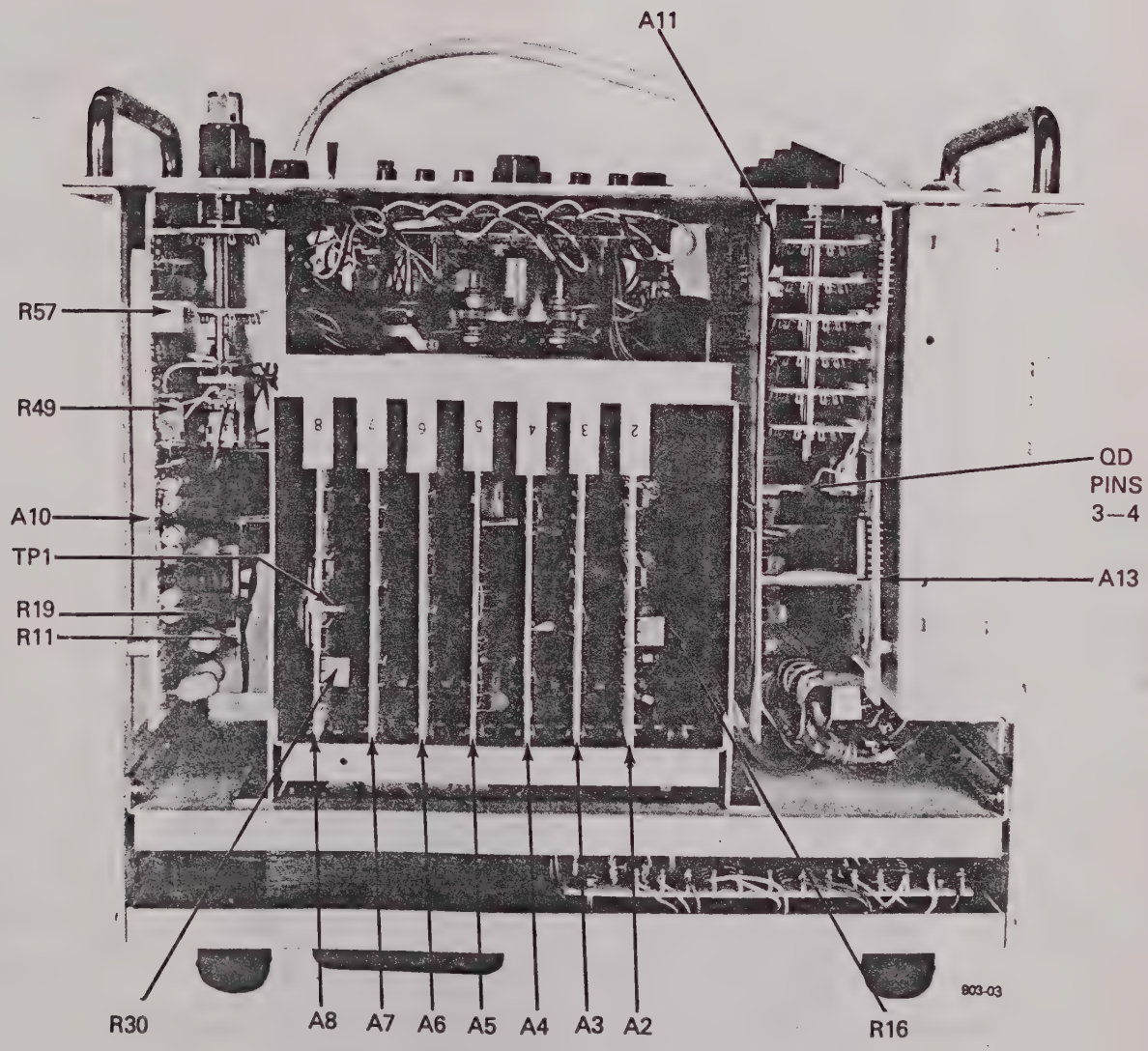

Figure 5—1. Model 7040 Top View Assembly and Adjustment Location.

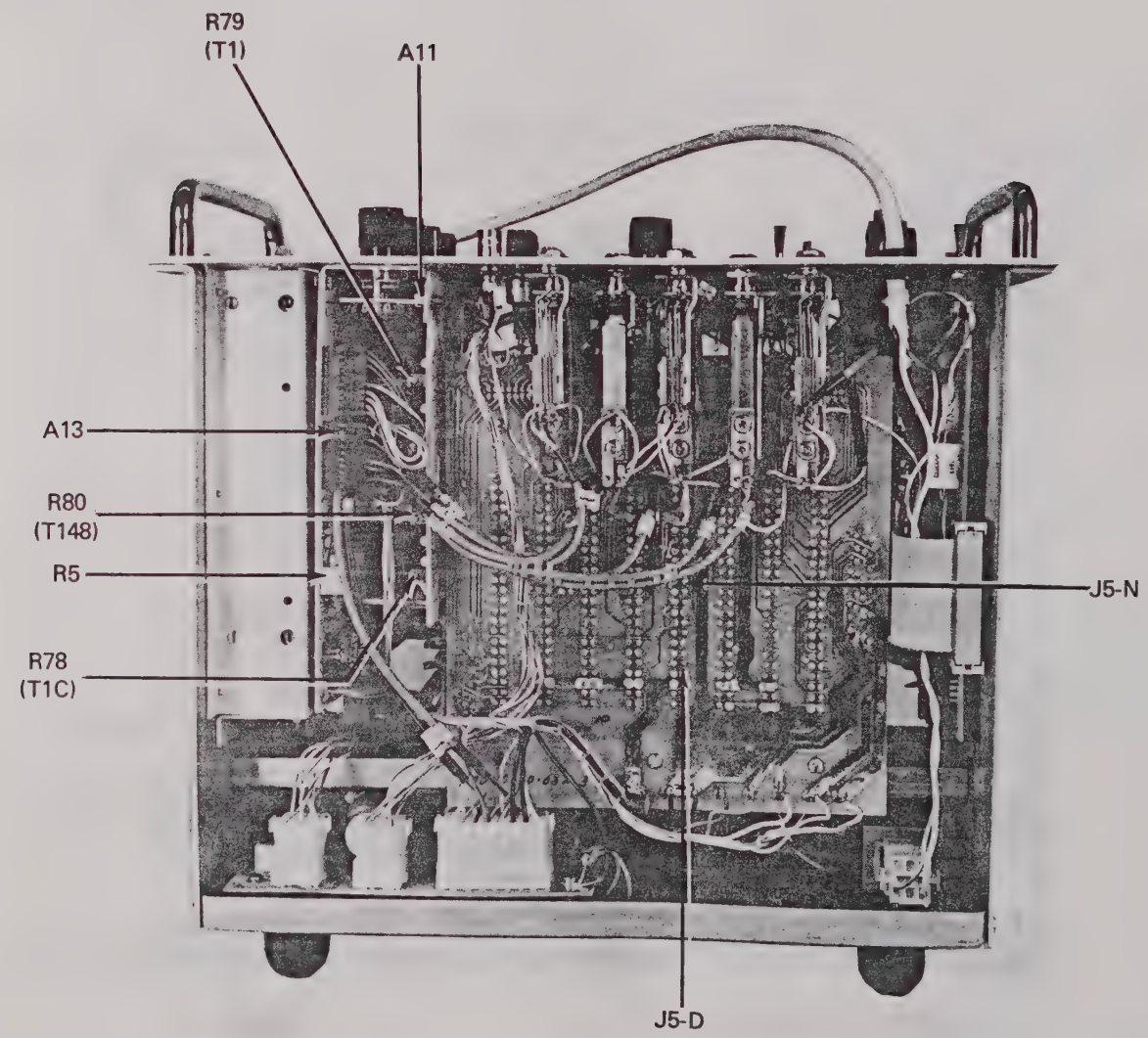

Figure 5—2. Model 7040 Bottom View Assembly and Adjustment Location.

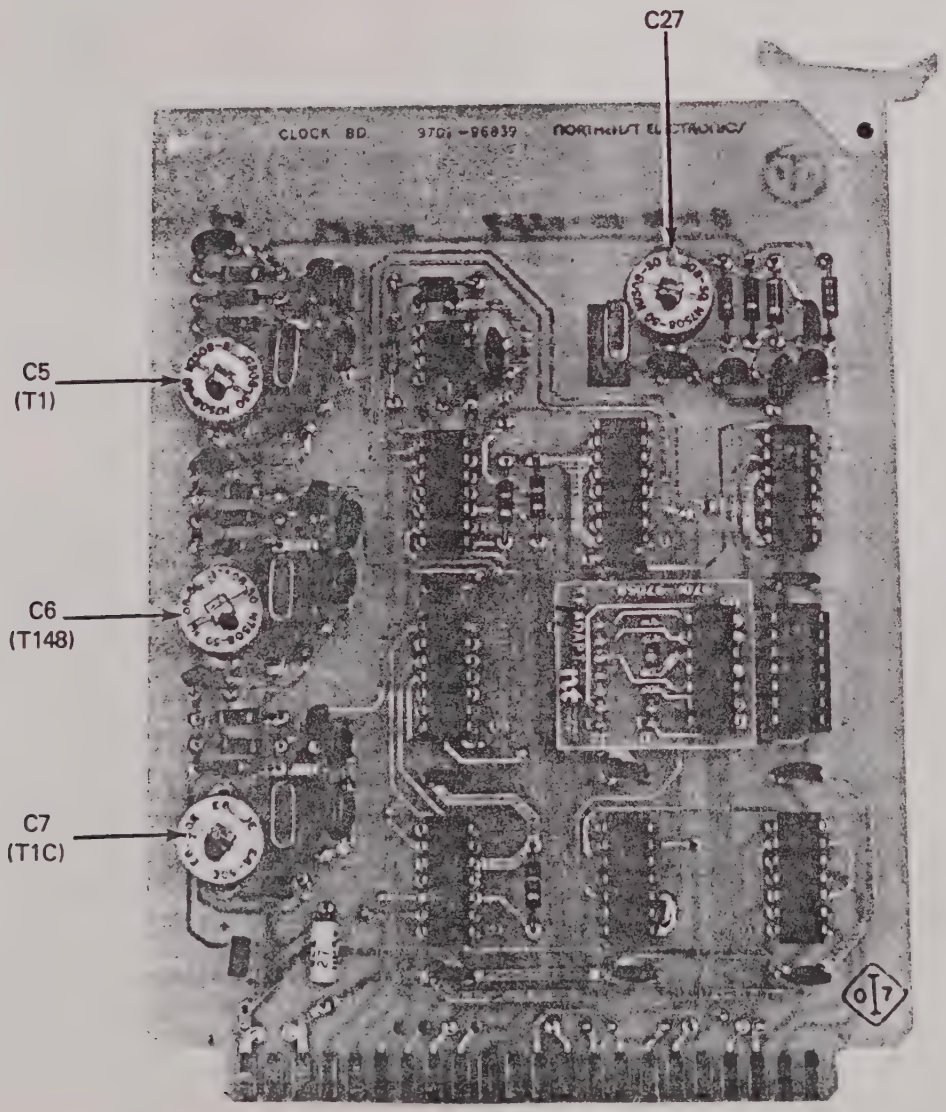

Figure 5—3. Model 7040 Clock Board A5 Adjustment Location.

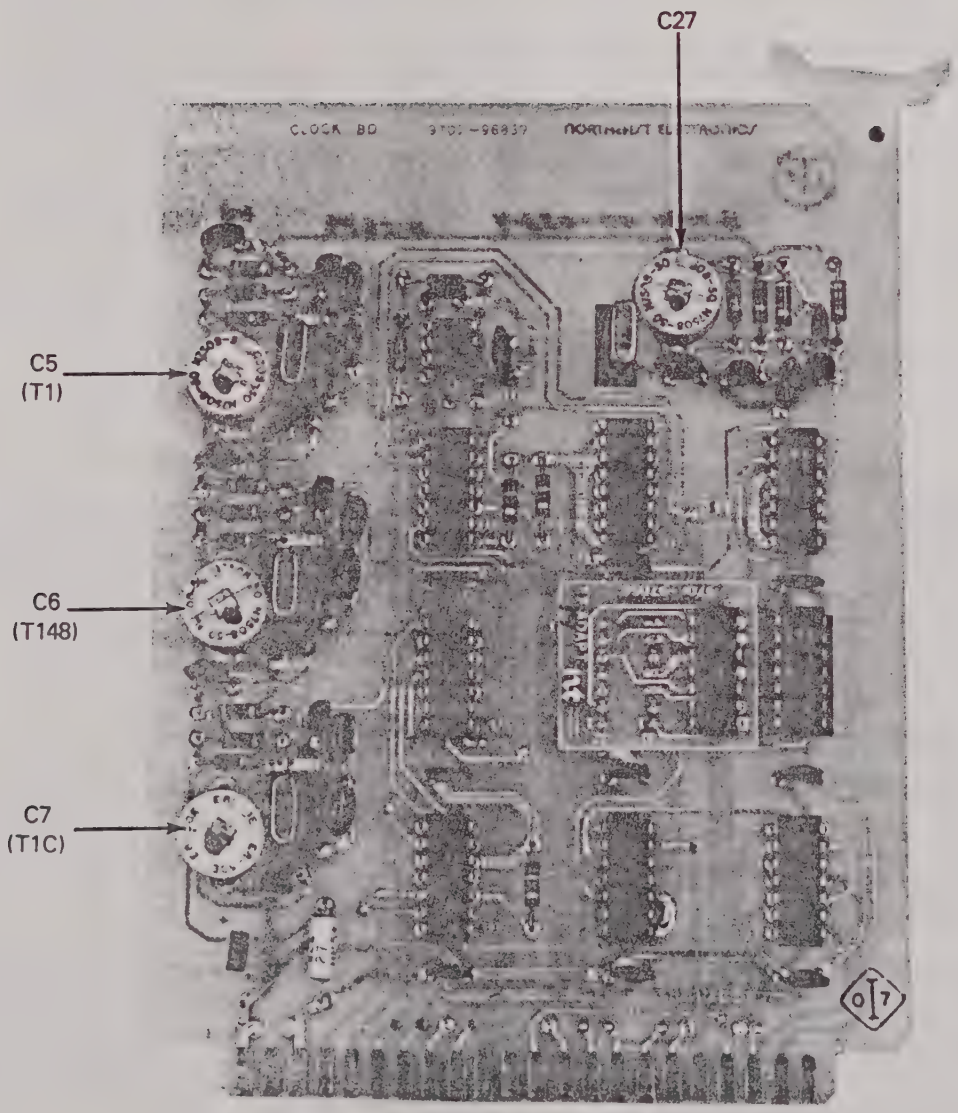

Figure 5—3. Model 7040 Clock Board A5 Adjustment Location.

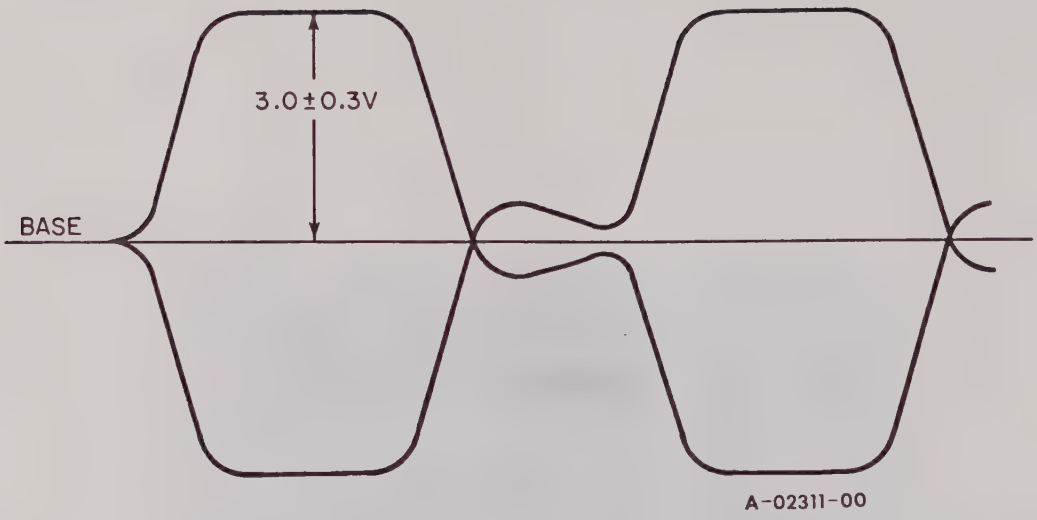

Figure 5—4. Model 7040 Generator Output Level Specification.

5.11 ALL ONES LEVEL ADJUSTMENT

5.12 This procedure is used to set the output level of the all ones generator. To adjust the all ones level, perform the following steps.

1. Remove the four front panel screws and the four rear panel screws and slide the cover off to the rear.

2. Wire a 100 ohm, 1% resistor across the tip and ring of a 310 plug.

3. Insert the plug and resistor combination into the GENERATOR OUT jack.

4. Connect the ac voltmeter input leads across the 100 ohm resistor.

5. Plug the 7040 power cord into an ac outlet.

6. Set the 7040 controls as follows:
   POWER switch to ON
   REPEATER TEST switch to 1 CABLE SIDE 1
   LINE LOSS dB switch to 5
   INTERFERENCE MARGIN dB switch to OFF
   SYSTEM switch to T1
   Function switch to ALL 1'S

7. Set the ac voltmeter controls to obtain a reference level indication. Record this reference level for future use.

8. Remove the ac voltmeter input leads from the 100 ohm resistor and remove the plug from the GENERATOR OUT jack.

9. Set the 7040 REPEATER TEST switch to 1 CABLE SIDE 2.

10. Set the 7040 POWER switch to OFF.

11. Remove Transmit Generator assembly A2 from the card cage. See Figure 5—2.

12. Insert the card extender into the card cage and plug A2 into the extender.

13. Place a 16-pin DIP IC test clip over transformer T1 on A2. See Figure 6—13 for the location of T1. The square solder connection is pin 1 on the transformer.

14. Connect the ac voltmeter input leads across pins 5 and 8 of T1 at the IC test clip.

15. Set the 7040 POWER switch to ON and set the REPEATER TEST switch to 1 CABLE SIDE 2.

16. The ac voltmeter indication should be within the range of 22 to 26 dB below the reference level recorded in step 7. If it is not, adjust R16 on A2 for an indication that is 24 dB below the reference level. See Figure 5—1.

17. Set the 7040 POWER switch to OFF and remove the ac power plug from the outlet.

18. Remove the ac voltmeter and the IC test clip.

19. Slide the cover on and replace the eight screws.

5.13 INTERFERENCE MARGIN LEVEL ADJUSTMENT

5.14 This procedure is used to set the interference signal level for T1, T1C, and T148. To make these adjustments, perform the following steps.

1. Remove the four front panel screws and the four rear panel screws and slide the cover off to the rear.

2. On A11, connect a 100 ohm, 1% resistor between quick disconnect pins 3 and 4. See Figure 5—1.

3. Connect the input leads of the ac voltmeter across the 100 ohm resistor.

4. Plug the 7040 power cord into an ac outlet.

5. Set the 7040 controls as follows:
   REPEATER TEST switch to 1 CABLE SIDE 1
   LINE LOSS dB switch to 31
   INTERFERENCE MARGIN dB switch to OFF
   SYSTEM switch to T1
   POWER switch to ON

6. Set the ac voltmeter controls to obtain a reference level indication. Record this reference level for future use.

7. Insert a dummy 310 plug into the 7040 GENERATOR OUT jack.

8. Set the 7040 INTERFERENCE MARGIN dB switch to 8.

9. The ac voltmeter indication should be within the range of 7.5 to 8.5 dB below the reference level recorded in step 6. If it is not, adjust R79 on A11 to obtain an indication that is 8 dB below the reference level of step 6. See Figure 5—2.

10. Set the 7040 controls as follows:
    INTERFERENCE MARGIN dB switch to OFF
    SYSTEM switch to T148

11. On the 7040, remove the dummy plug from the GENERATOR OUT jack.

12. Set the ac voltmeter controls to obtain a reference level indication. Record this reference level for future use.

13. On the 7040, set the INTERFERENCE MARGIN dB switch to 8 and insert the dummy 310 plug into the GENERATOR OUT jack.

14. The ac voltmeter indication should be within the range of 7.5 to 8.5 dB below the reference level of step 12. If it is not, adjust R80 on A11 to obtain an indication that is 8 dB below the reference level of step 12. See Figure 5—2.

15. Set the 7040 controls as follows:
    INTERFERENCE MARGIN dB switch to OFF
    SYSTEM switch to T1C

16. On the 7040, remove the dummy plug from the GENERATOR OUT jack.

17. Set the ac voltmeter controls to obtain a reference level indication. Record this reference level for future use.

18. On the 7040, set the INTERFERENCE MARGIN dB switch to 8 and insert the dummy 310 plug into the GENERATOR OUT jack.

19. The ac voltmeter indication should be within the range of 7.5 to 8.5 dB below the reference level of step 17. If it is not, adjust R78 on A11 to obtain an indication that is 8 dB below the reference level of step 17. See Figure 5—2.

20. Set the 7040 POWER switch to OFF and remove the power cord from the ac outlet.

21. Remove the ac voltmeter input leads and the 100 ohm resistor from pins 3 and 4 on A11.

22. Slide the cover on and replace the eight screws.

5.15 ANALOG FAULT LOCATE RECEIVER AND C-MESSAGE FILTER ADJUSTMENTS

5.16 This procedure is used to adjust the common input attenuator, the QRMS detector, and the C-message filter. To make these adjustments, perform the following steps.

1. Remove the four front panel screws and the four rear panel screws and slide the cover off to the rear.

2. As shown on Figure 5—5, connect the ac voltage calibrator, frequency counter, 600 ohm buildout resistor, 600 ohm H attenuator, and the Model 7040 into the test configuration. See Figure 5—1 for the location of TP1 on A8.

3. Plug the 7040 power cord into an ac outlet.

4. Set the 7040 controls as follows:
   Function switch to MEAS 1
   LINE FILTER switch to M
   PULSE PERIOD switch to REF
   FAULT LOCATE RECEIVE LEVEL switch to −50 dB
   Variable sensitivity fully clockwise to CAL
   FAULT LINE switch to LEVEL
   POWER switch to ON

5. Set the H attenuator to 20 dB.

6. On the ac voltage calibrator, set the frequency to 1000 Hz, the output level to 50.000 millivolts rms, and the phase lock switch to OFF.

7. Set the ac voltmeter controls to obtain an on scale indication. Record this reference level for future use.

8. Set the 7040 FAULT LOCATE RECEIVE LEVEL dBm switch to −40 dB.

9. On the ac voltage calibrator, set the output level to 0.158114 volts rms.

10. The ac voltmeter indication should be the same as the level recorded in step 7 ± 0.1 dB. If it is not, adjust R57 on A10 to obtain an indication that is the same as the level recorded in step 7. See Figure 5−1.

NOTE

If R57 is adjusted, all of the other adjustments on the Analog Fault Locate assembly will have to be readjusted. R57 is common to both the C-message filter and the analog fault locate receiver.

11. On the 7040, set the LINE FILTER switch to F and the FAULT LOCATE RECEIVE LEVEL dBm switch to 0 dB.

12. On the ac voltage calibrator, set the frequency to 1508 Hz, the level to 1.58114 volts rms, and set the phase lock switch to ON.

13. Set the H attenuator to 0 dB.

14. On A10, adjust R19 to obtain an indication of 0 dBm on the 7040 front panel meter. See Figure 5−1.

15. Set the H attenuator to 10 dB.

16. On A10, adjust R11 to obtain an indication of −10 dBm on the front panel meter. See Figure 5−1.

17. Repeat steps 13 through 16 until no further adjustments are required to obtain indications of exactly 0 dBm and −10 dBm when the H attenuator is changed by 10 dB.

18. Set the 7040 controls as follows:

   Function switch to STOP XMT
   FAULT LOCATE RECEIVE LEVEL dBm switch to −10 dB
   FAULT LINE switch to NOISE

19. On the ac voltage calibrator, set the frequency to 1000 Hz, the level to 0.5000 volts rms, and set the phase lock switch to OFF.

20. Set the H attenuator to 0 dB.

21. The 7040 front panel meter should indicate between −9.5 dBm and −10.5 dBm. If it does not, adjust R49 on A10 for an indication of −10 dBm. See Figure 5−1.

22. Set the 7040 POWER switch to OFF and remove the ac power plug.

23. Remove all test equipment.

24. Slide the cover on and replace the eight screws.

5.17 PULSE PERIOD SWITCHING DURATION ADJUSTMENT

5.18 This procedure is used to set the length of time spent at each pulse period during auto cycling. To adjust this time, perform the following steps.

1. Remove the four front panel screws and the four rear panel screws and slide the cover off to the rear.

2. Plug the 7040 ac power plug into an ac outlet.

3. Set the POWER switch to ON.

4. Momentarily set the PULSE PERIOD switch to REF and then to AUTO. As the cycling stops at each pulse period number, the associated indicator will be lighted. To change this time, adjust R30 on A8 to obtain the desired time. The time can be set within the range of approximately 1 second to 10 seconds.

5. Set the POWER switch to OFF and remove the ac power plug.

6. Slide the cover on and replace the eight screws.

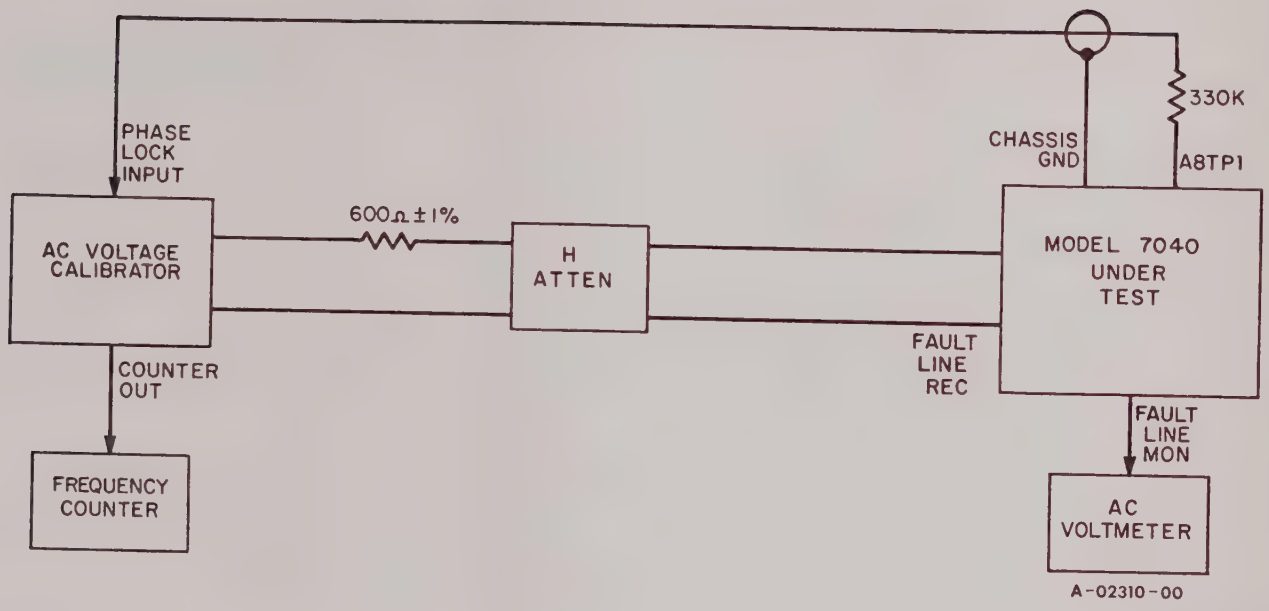

Figure 5—5. Model 7040 Analog Fault Locate Assembly Calibration Test Setup.

SECTION 6

DIAGRAMS

6.1 This section contains the functional schematic diagrams, schematic diagrams, and the parts location diagrams for the Model 7040.

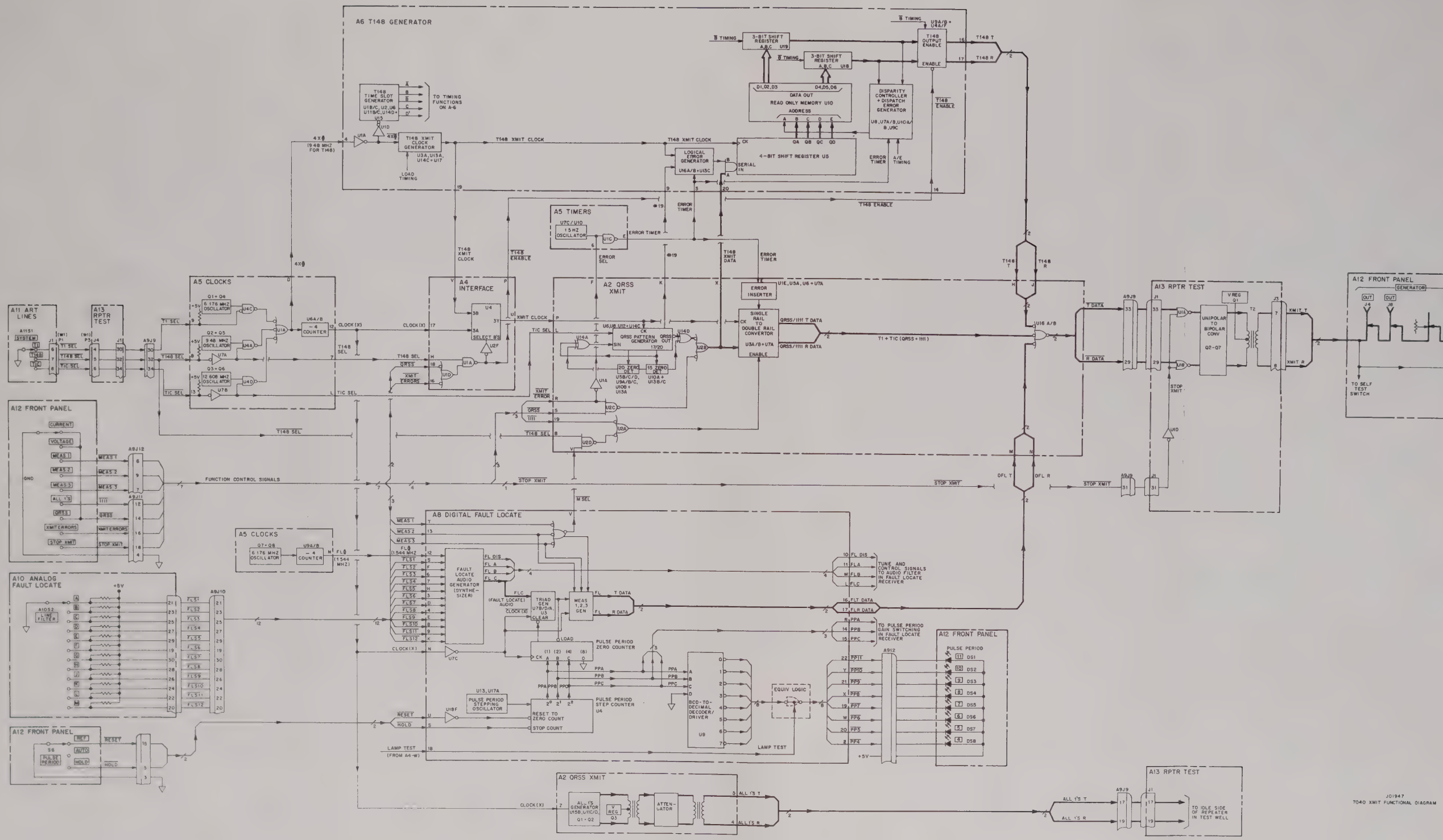

Figure 6—1. 7040 Transmit Section Functional Diagram

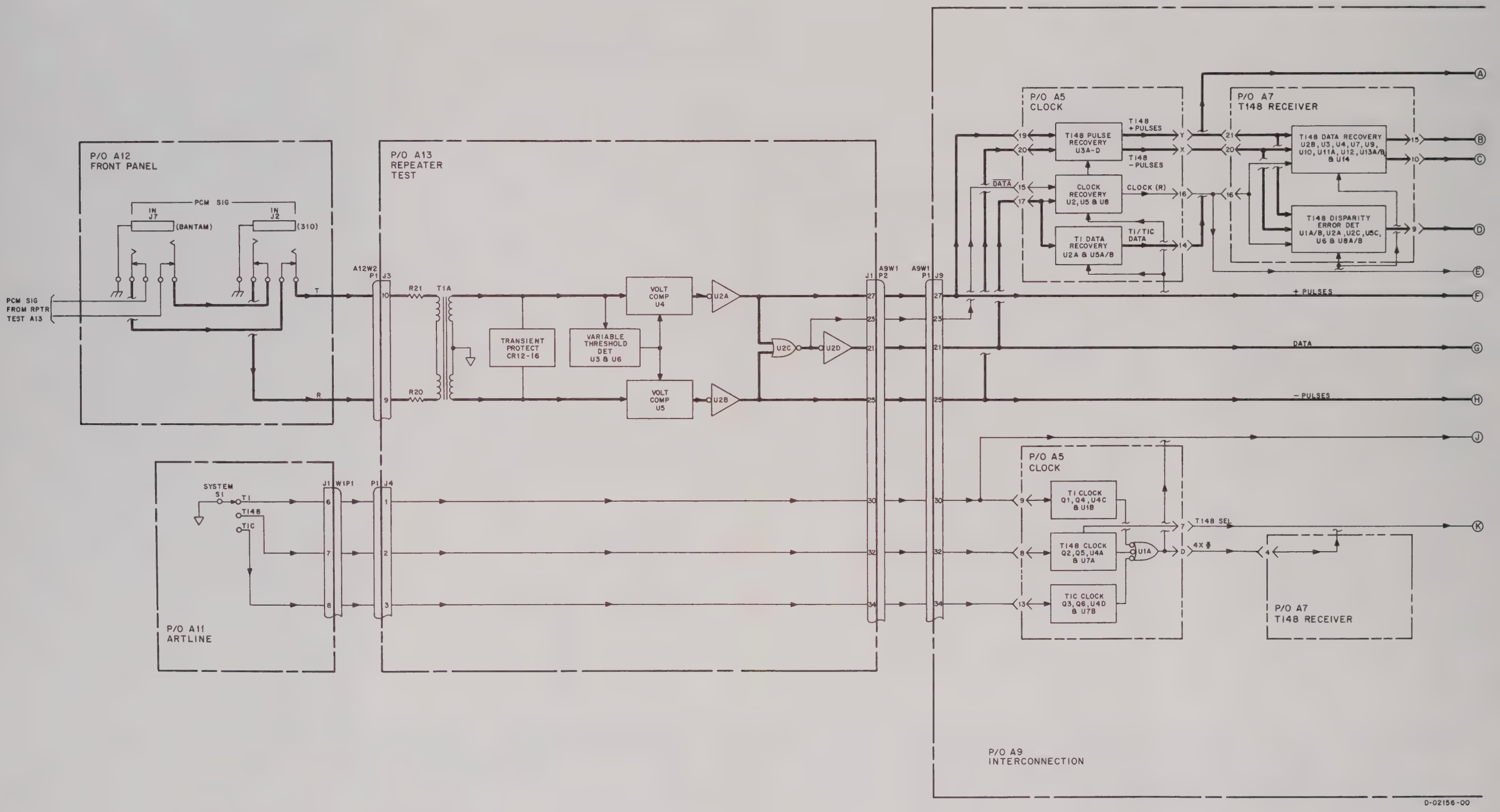

Figure 6—2. 7040 PCM Receiver Section Functional Diagram [Sheet 1 of 2]

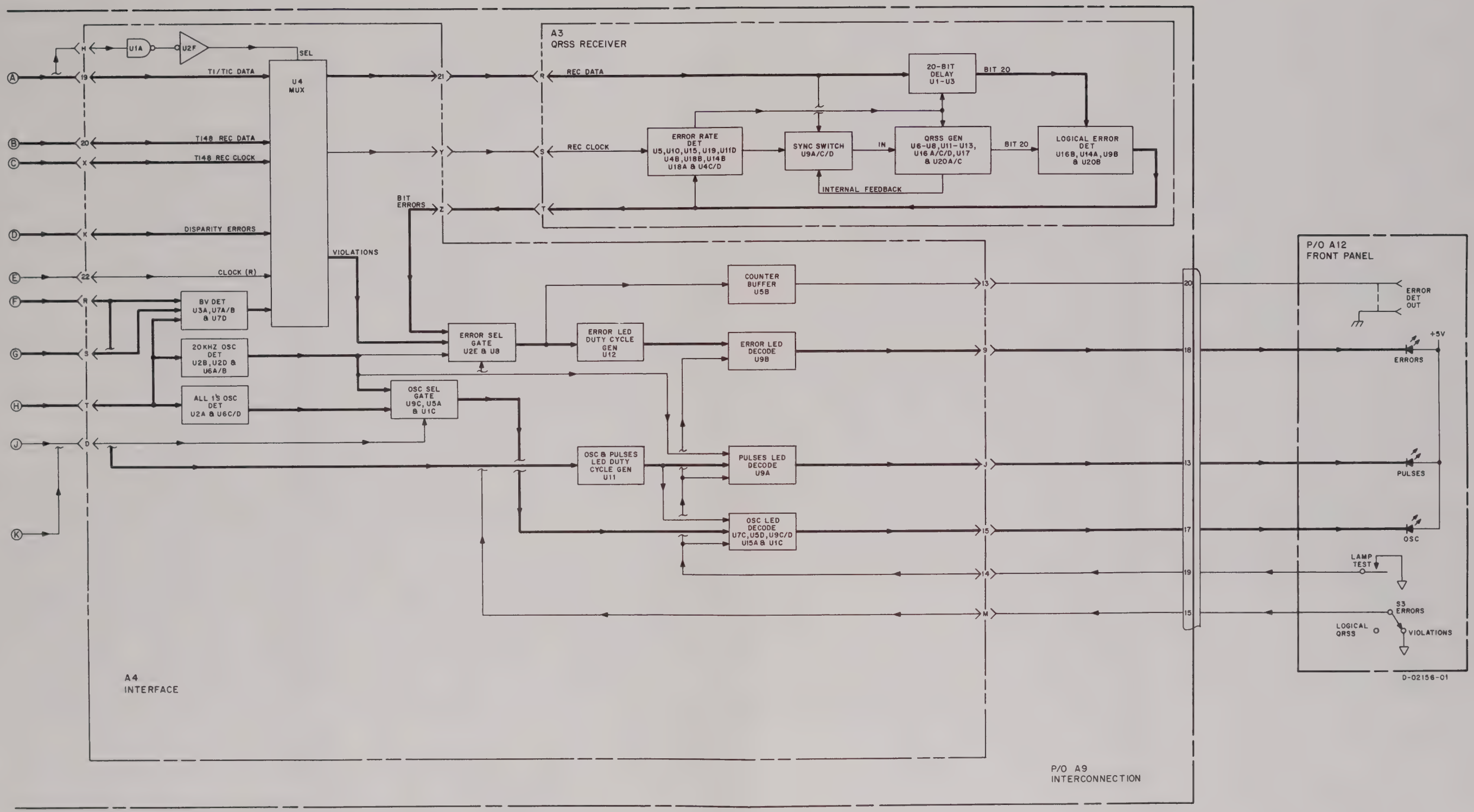

Figure 6—2. 7040 PCM Receiver Section Functional Diagram [Sheet 2 of 2]

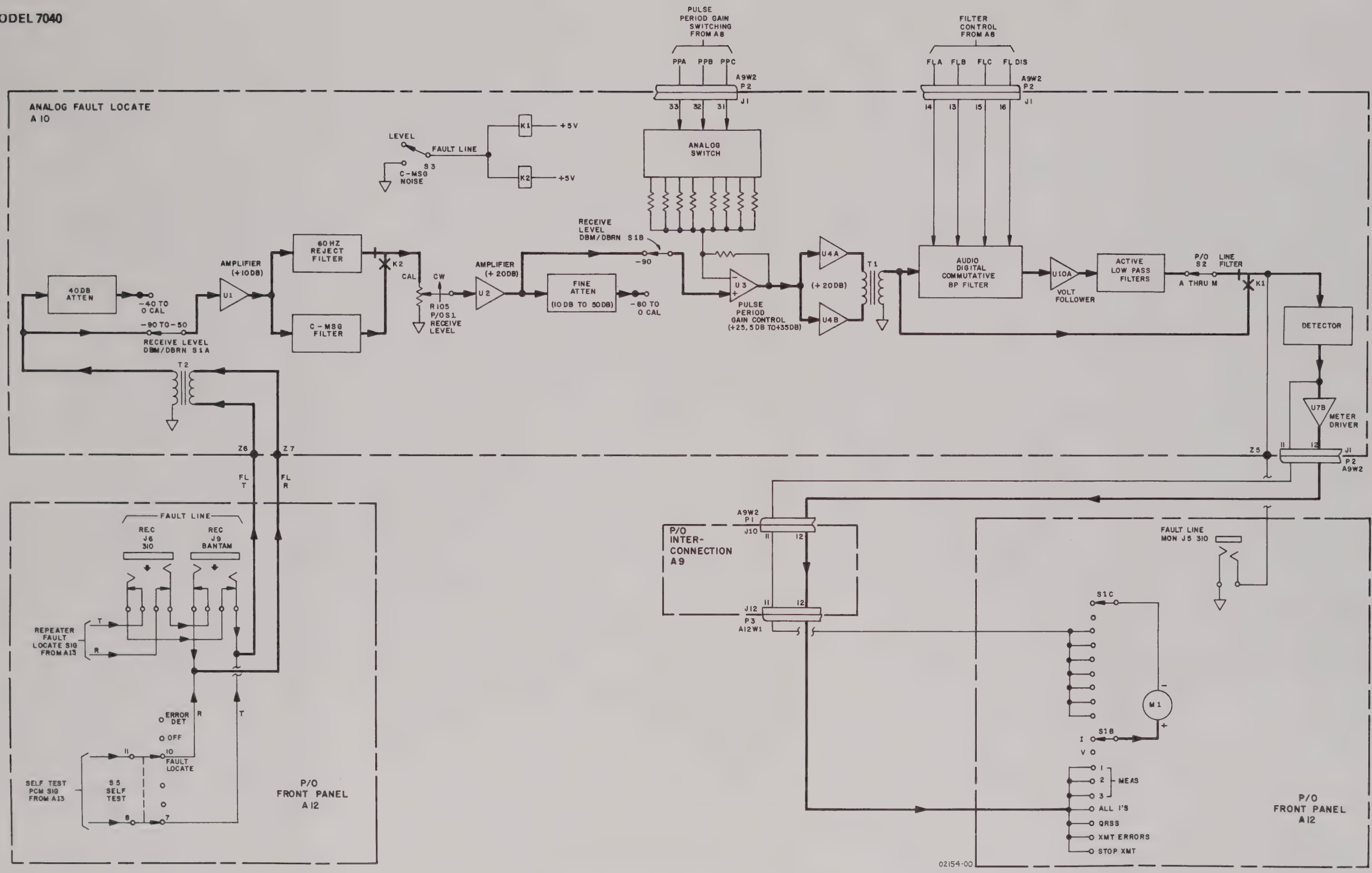

Figure 6—3. Analog Fault Locate Receiver Functional Diagram

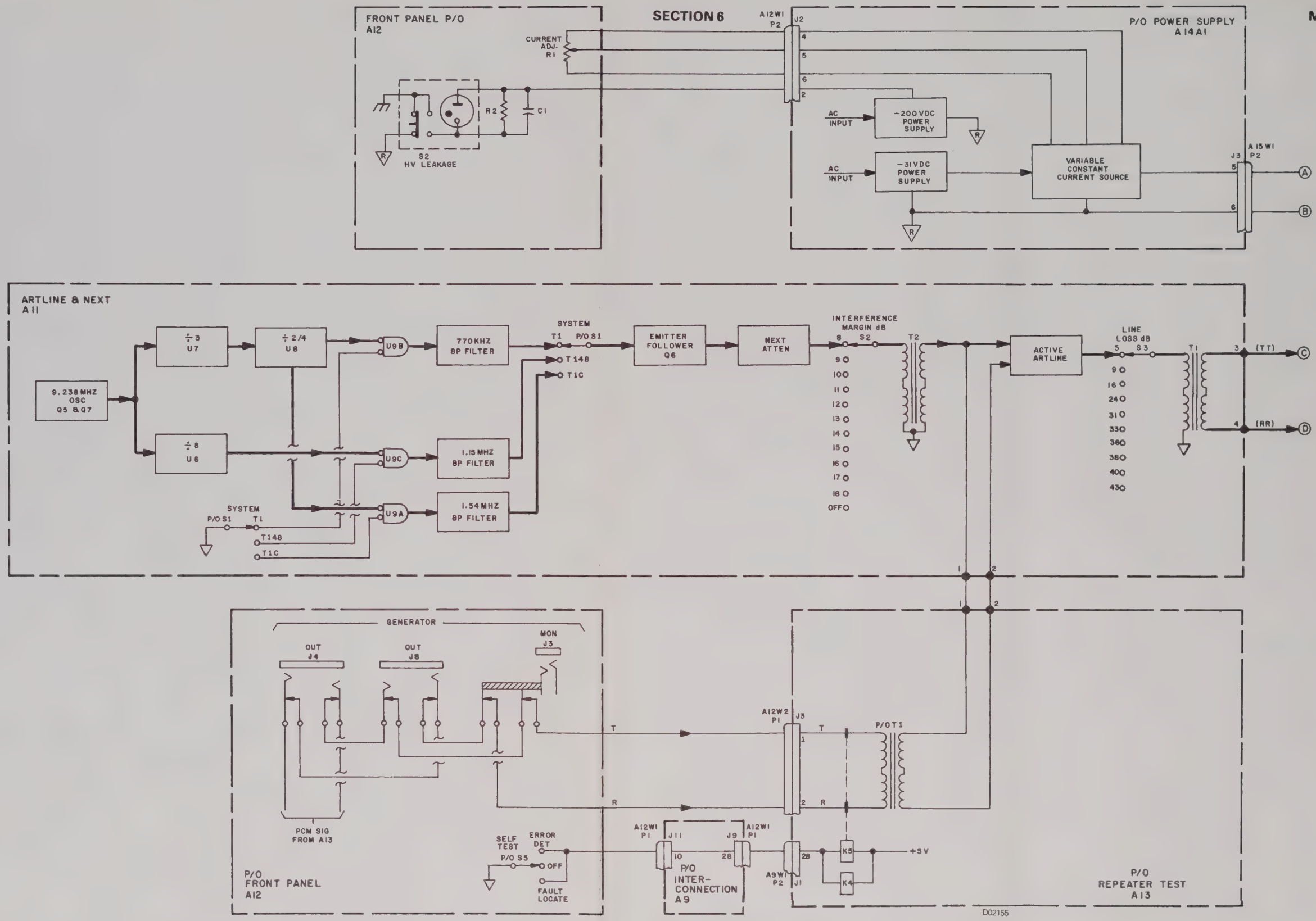

Figure 6—4. Repeater Test Section Functional Diagram [Sheet 1 of 2]

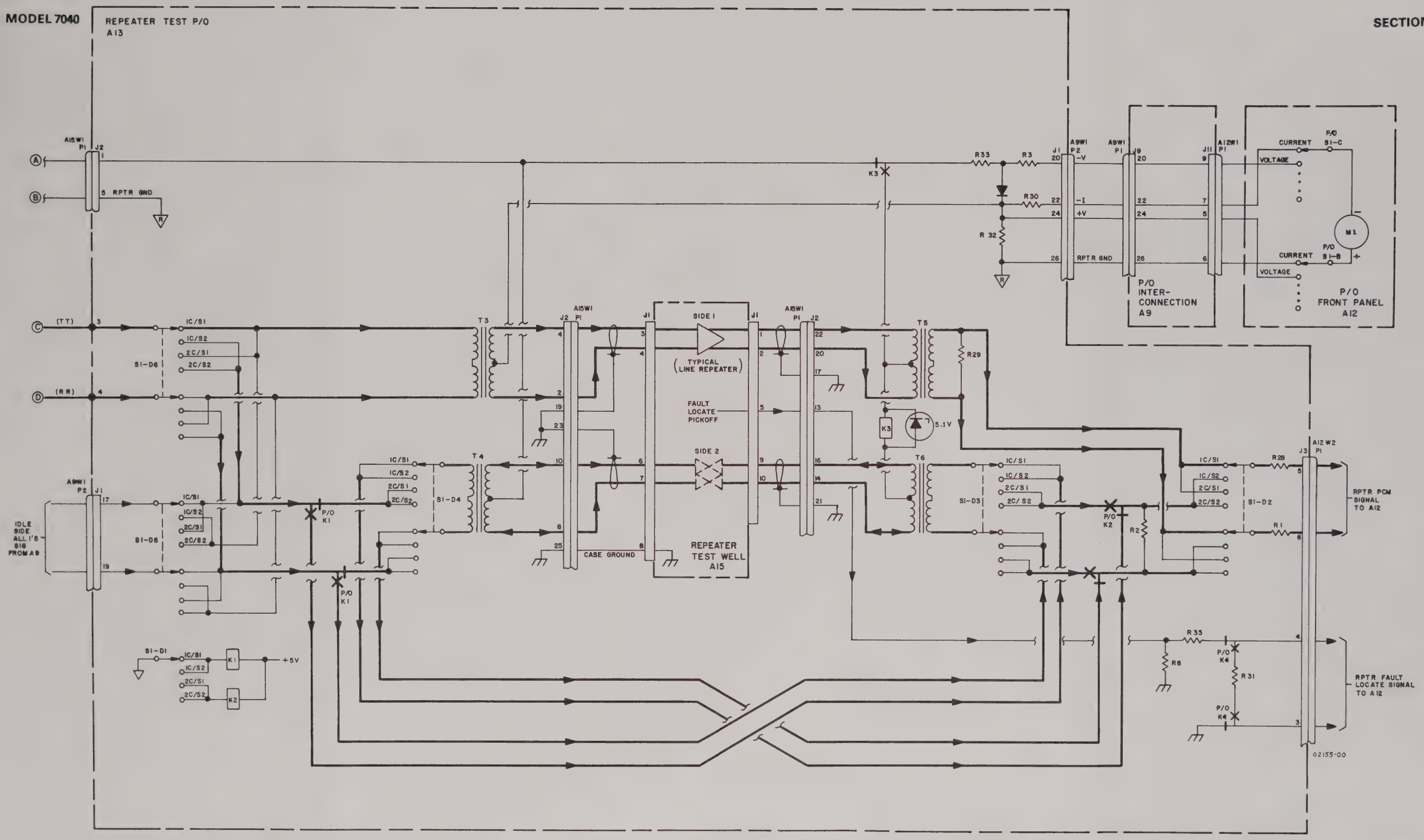

Figure 6—4. Repeater Test Section Functional Diagram [Sheet 2 of 2]

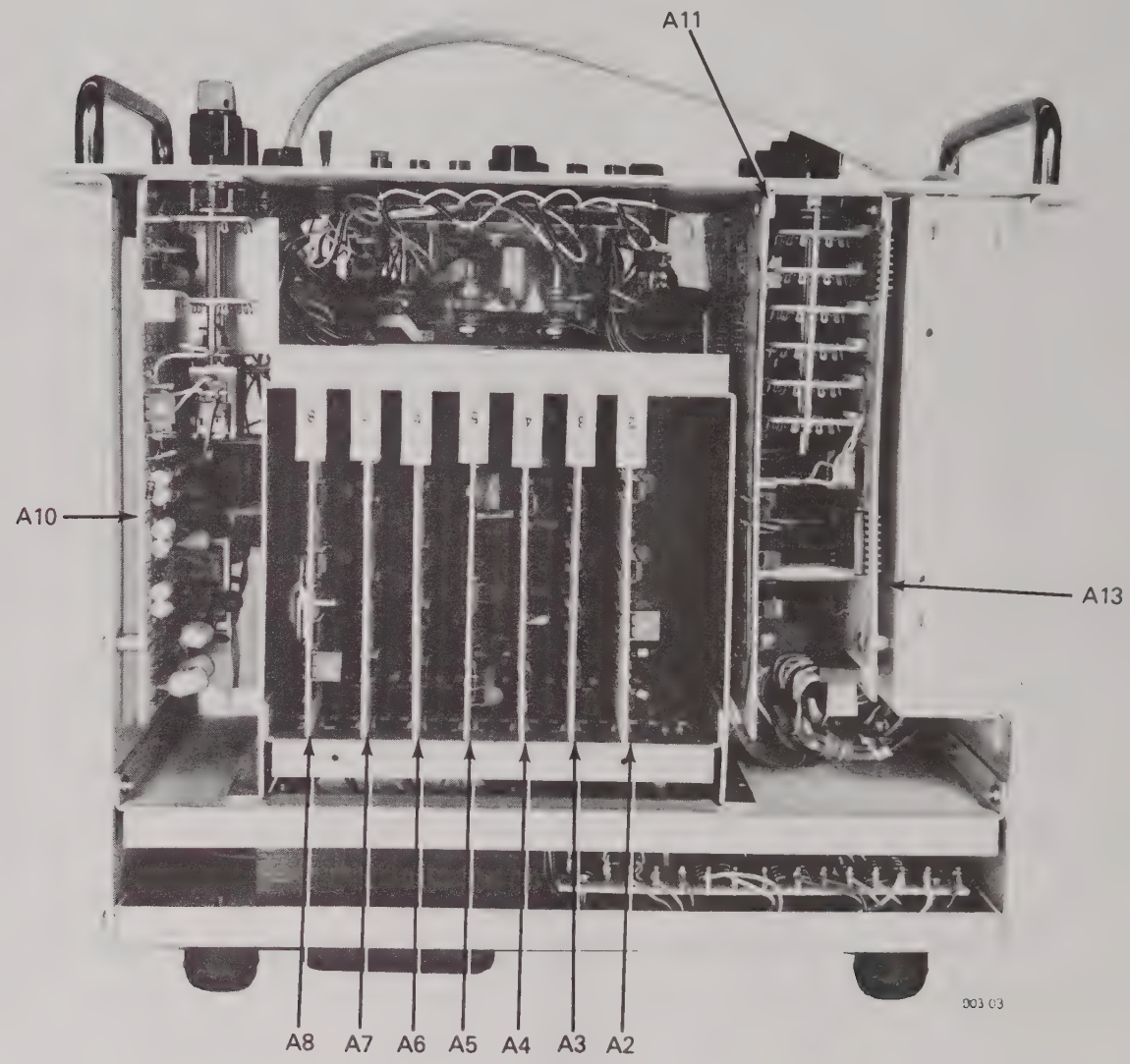

Figure 6—5. 7040 Overall Assembly Location

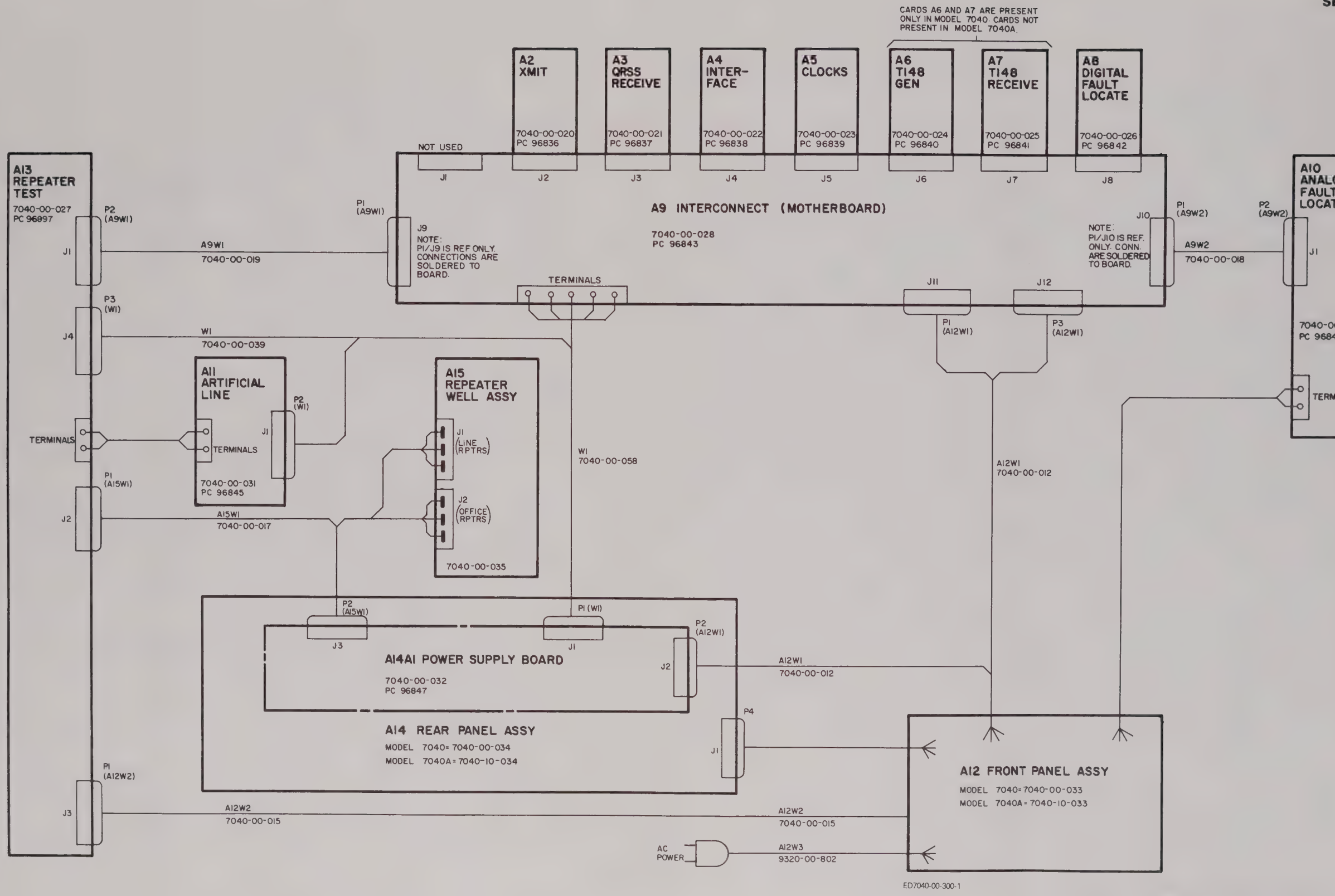

Figure 6—6. 7040 Intercabling Diagram

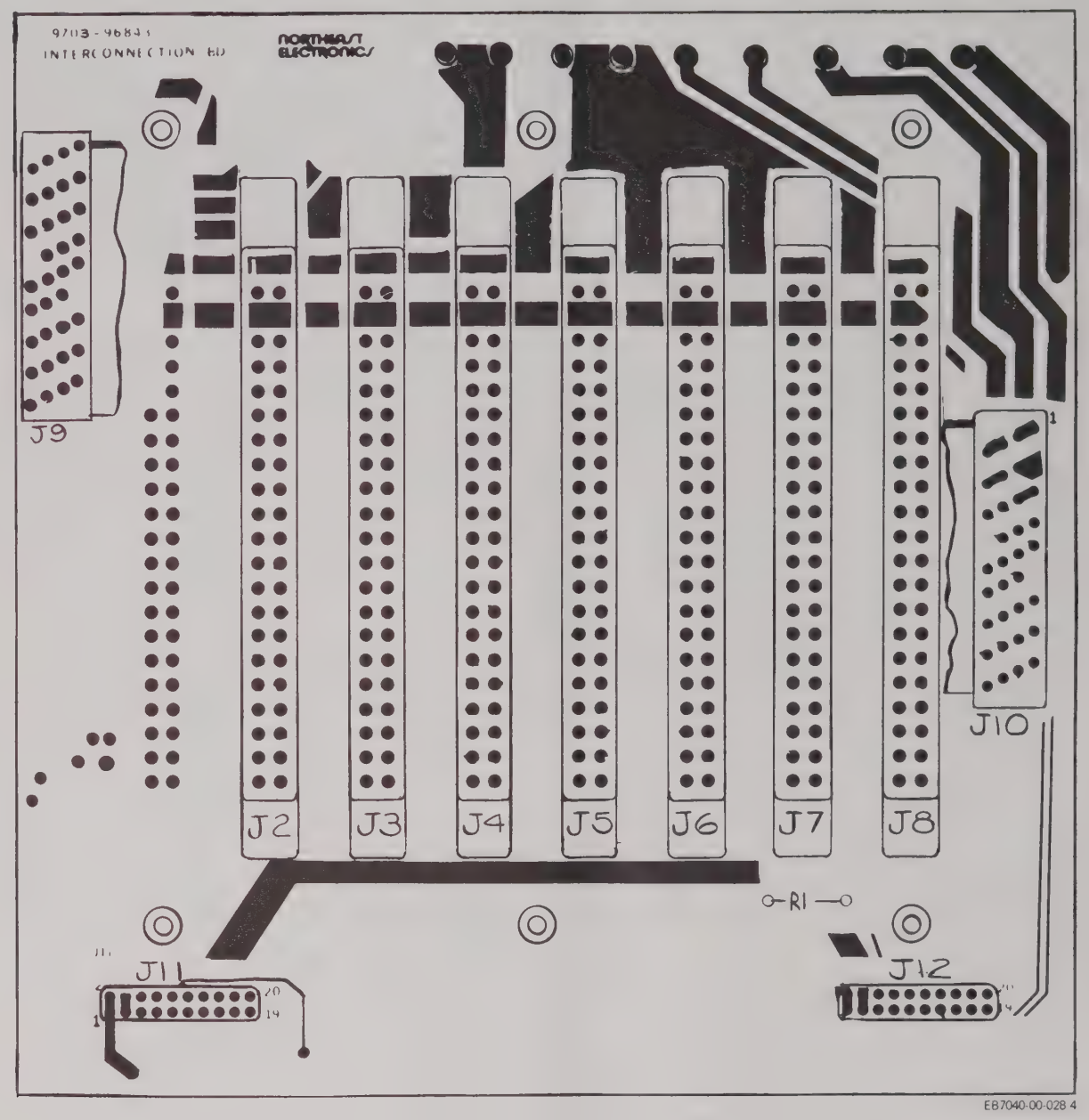

Figure 6—7. 7040 Interconnection Assembly A9 Parts Location Diagram

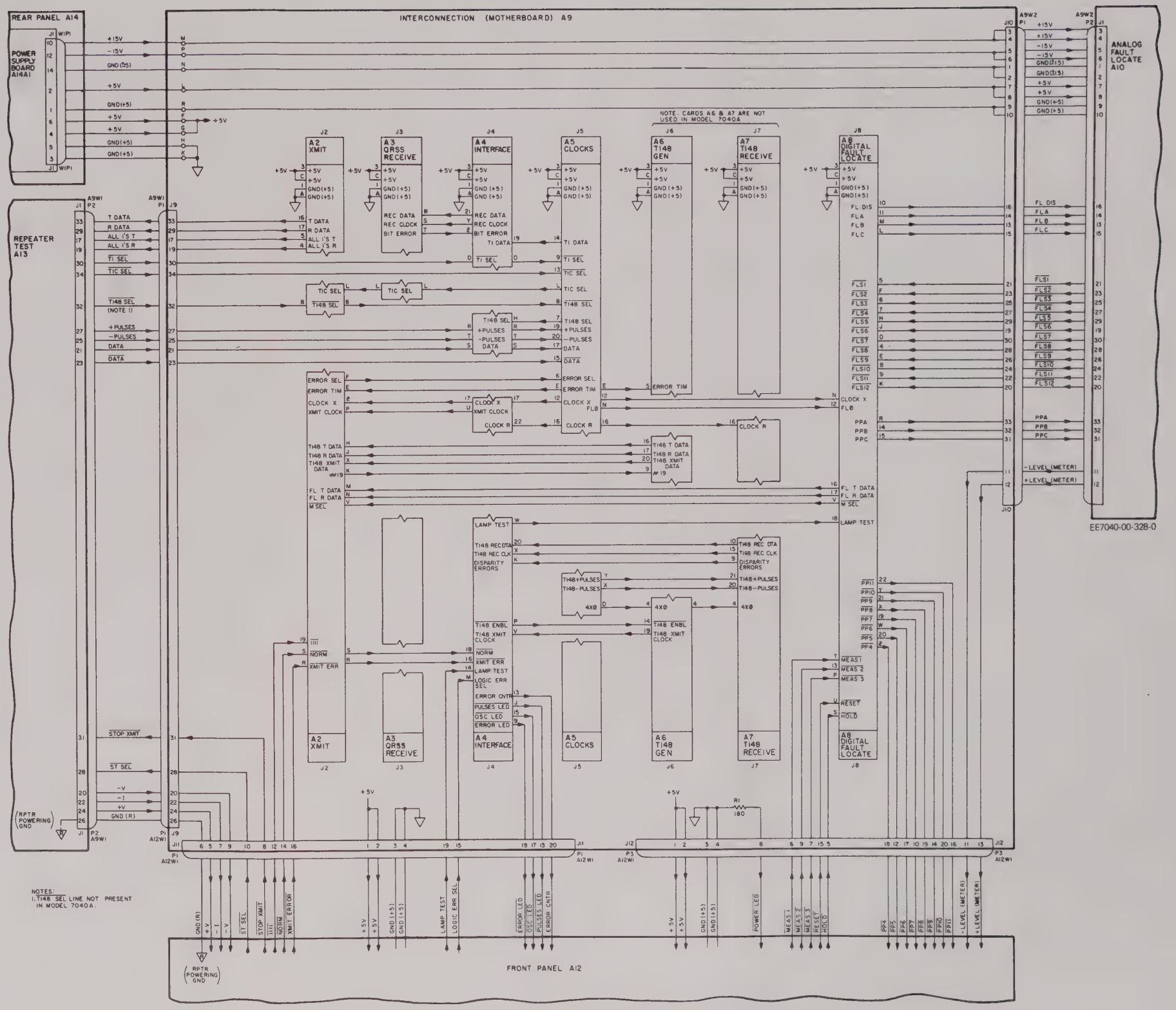

Figure 6—8. 7040 Interconnection Assembly A9 Schematic Diagram

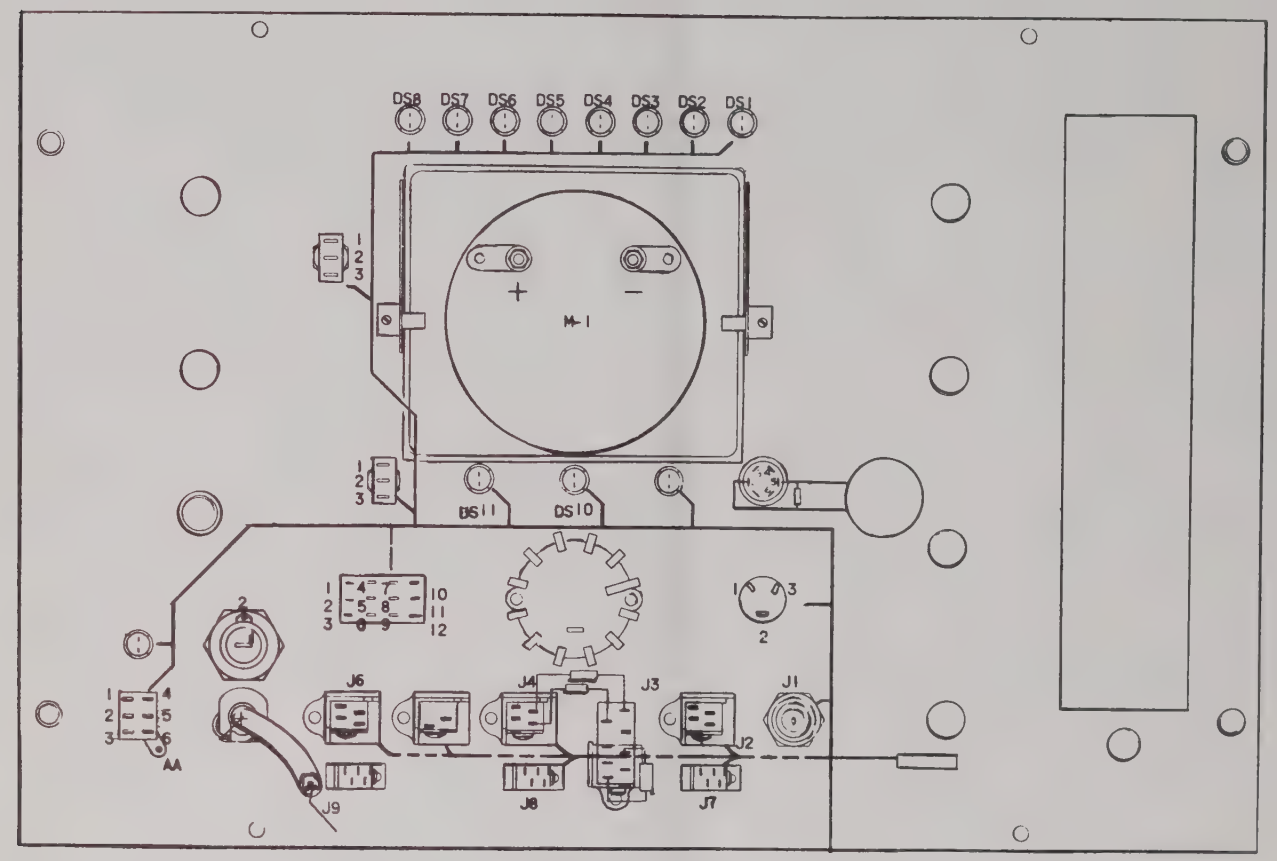

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Figure 6—9. 7040 Front Panel Assembly A12 Parts Location Diagram

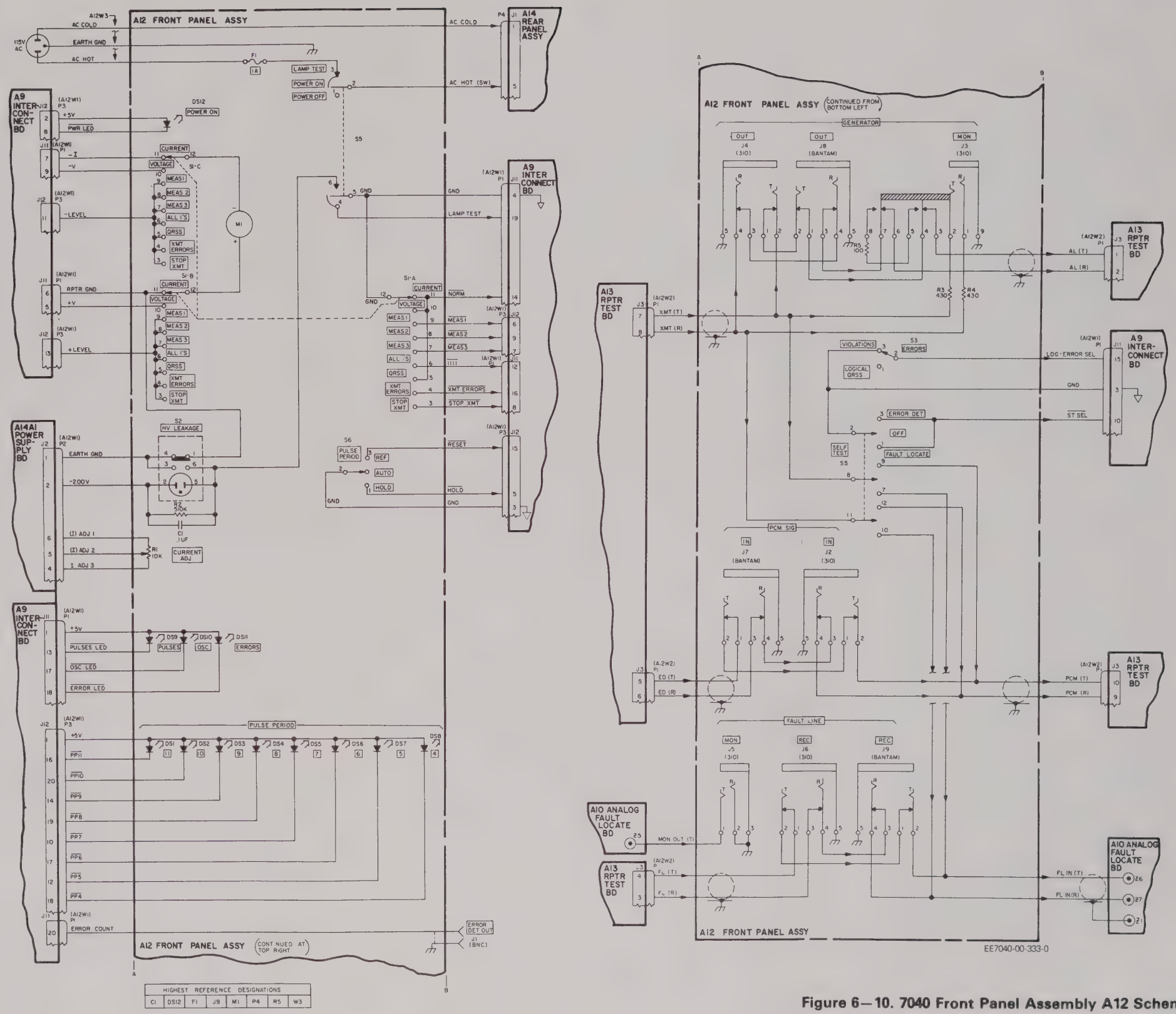


Figure 6—10. 7040 Front Panel Assembly A12 Schematic Diagram

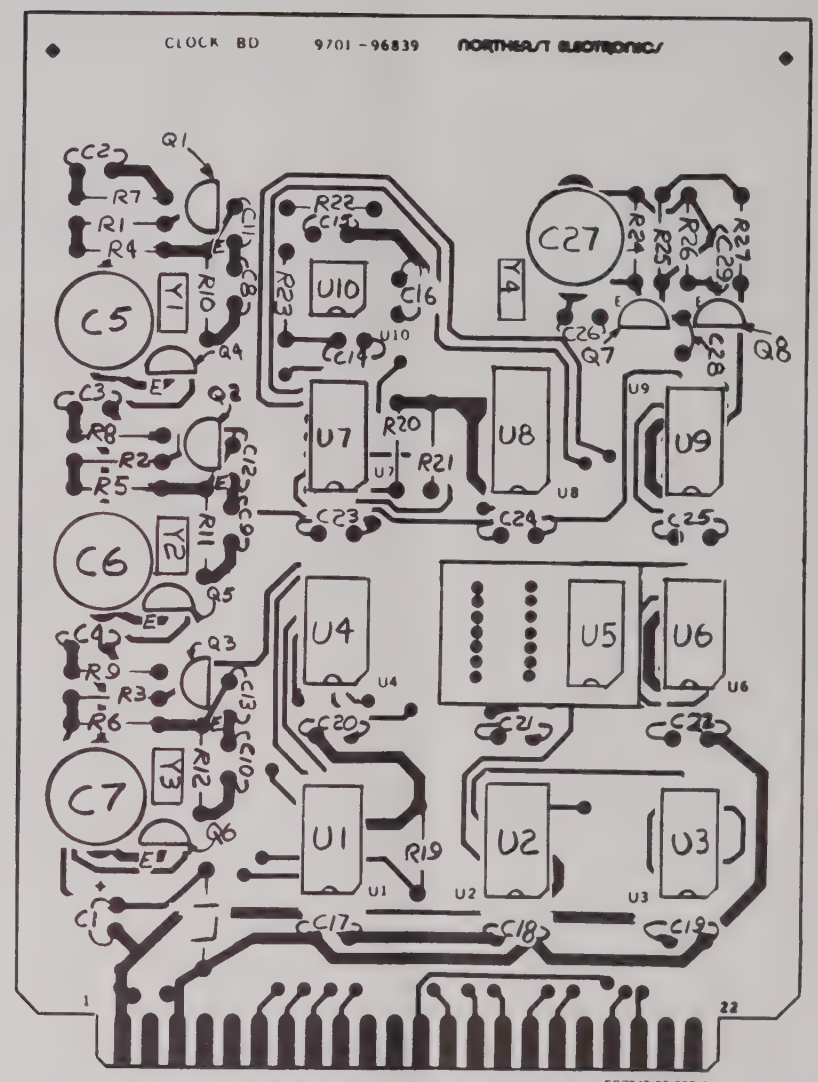
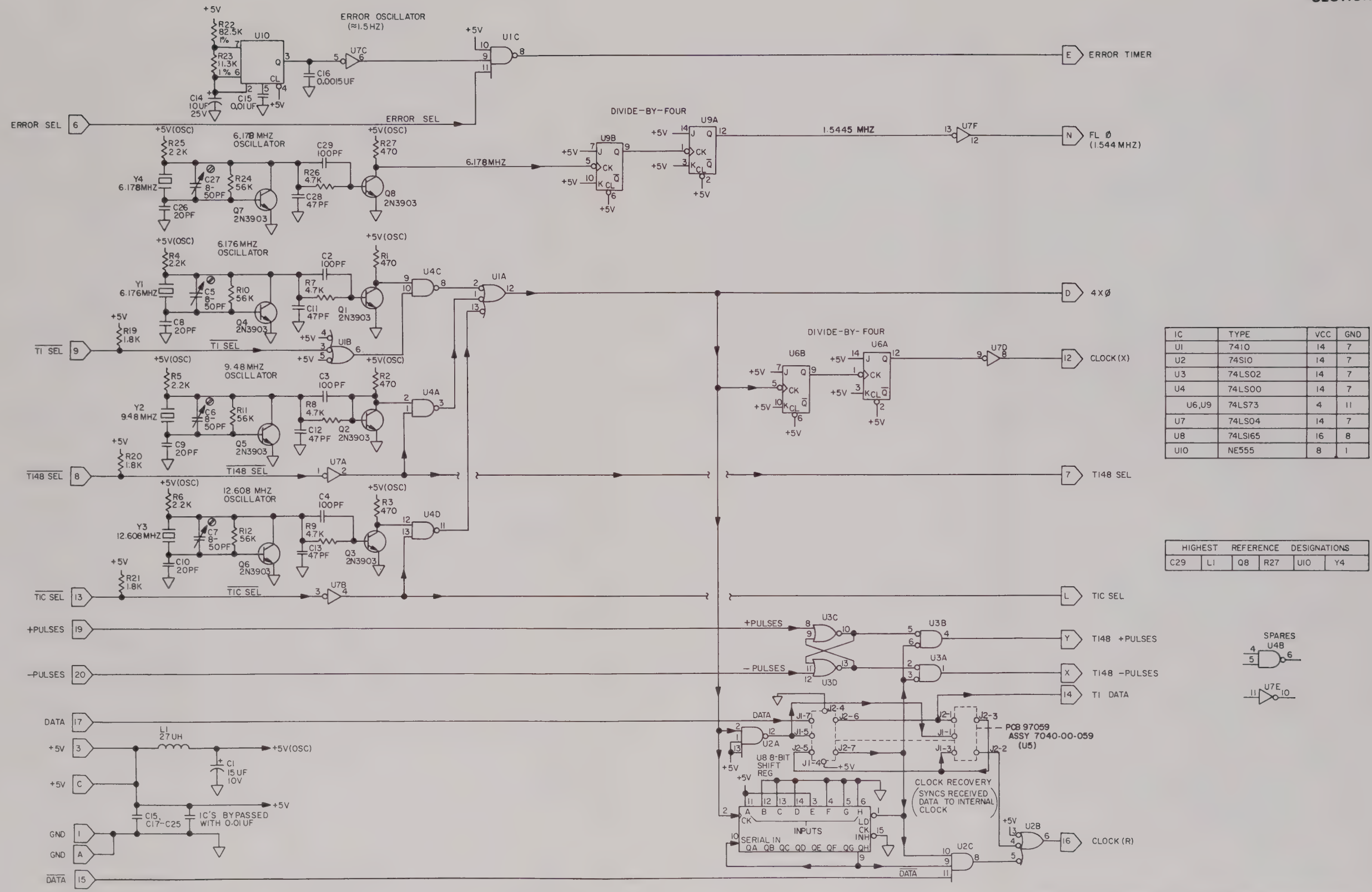


Figure 6—11. 7040 Clock Assembly A5 Parts Location Diagram



IC	TYPE	VCC	GND
U1	7410	14	7
U2	74S10	14	7
U3	74LS02	14	7
U4	74LS00	14	7
U6,U9	74LS73	4	11
U7	74LS04	14	7
U8	74LS165	16	8
U10	NE555	8	1

HIGHEST REFERENCE DESIGNATIONS					
C29	L1	Q8	R27	U10	Y4

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Figure 6—12. 7040 Clock Assembly A5 Schematic Diagram

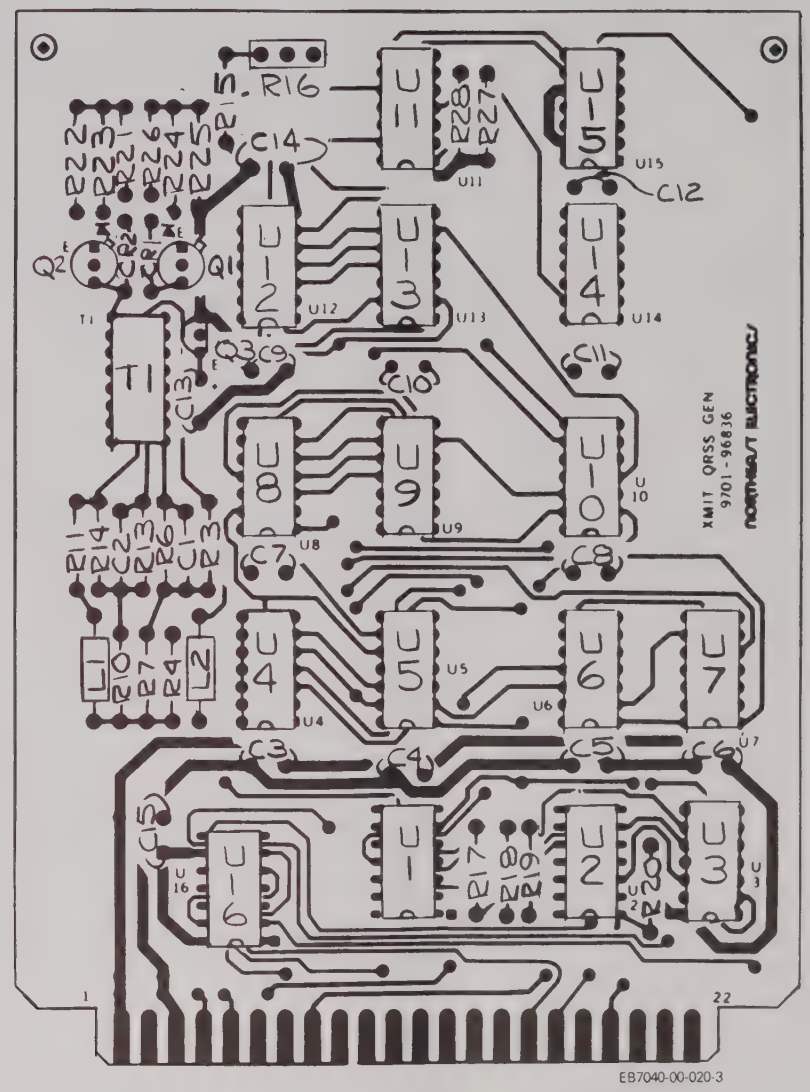
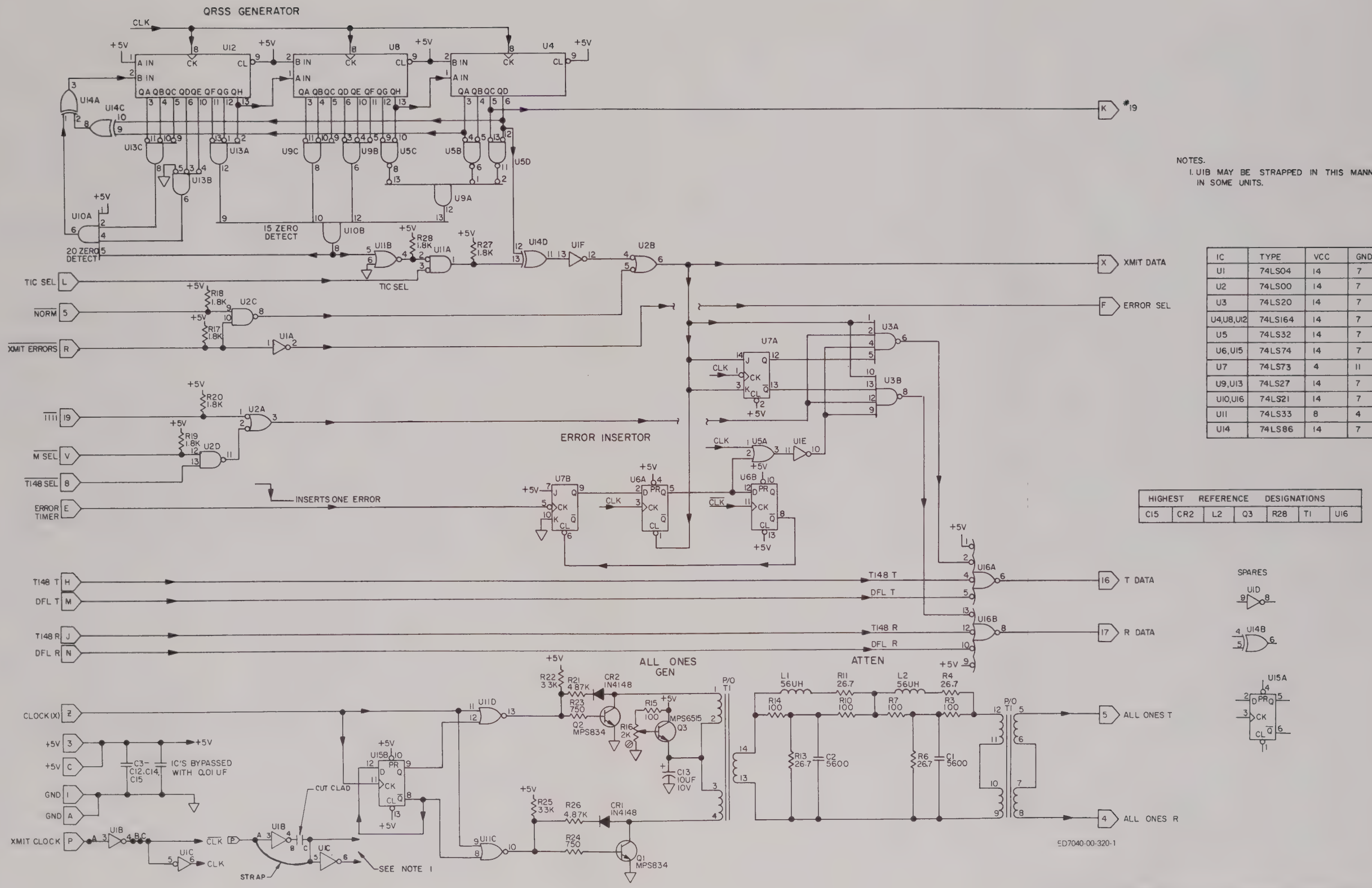


Figure 6—13. 7040 Transmit Generator Assembly A2 Parts Location Diagram



NOTES.
1. U1B MAY BE STRAPPED IN THIS MANNER IN SOME UNITS.

IC	TYPE	VCC	GND
U1	74LS04	14	7
U2	74LS00	14	7
U3	74LS20	14	7
U4,U8,U12	74LS164	14	7
U5	74LS32	14	7
U6,U15	74LS74	14	7
U7	74LS73	4	11
U9,U13	74LS27	14	7
U10,U16	74LS21	14	7
U11	74LS33	8	4
U14	74LS86	14	7

HIGHEST REFERENCE DESIGNATIONS						
C15	CR2	L2	Q3	R28	T1	U16

Figure 6—14. 7040 Transmit Generator Assembly A2 Schematic Diagram

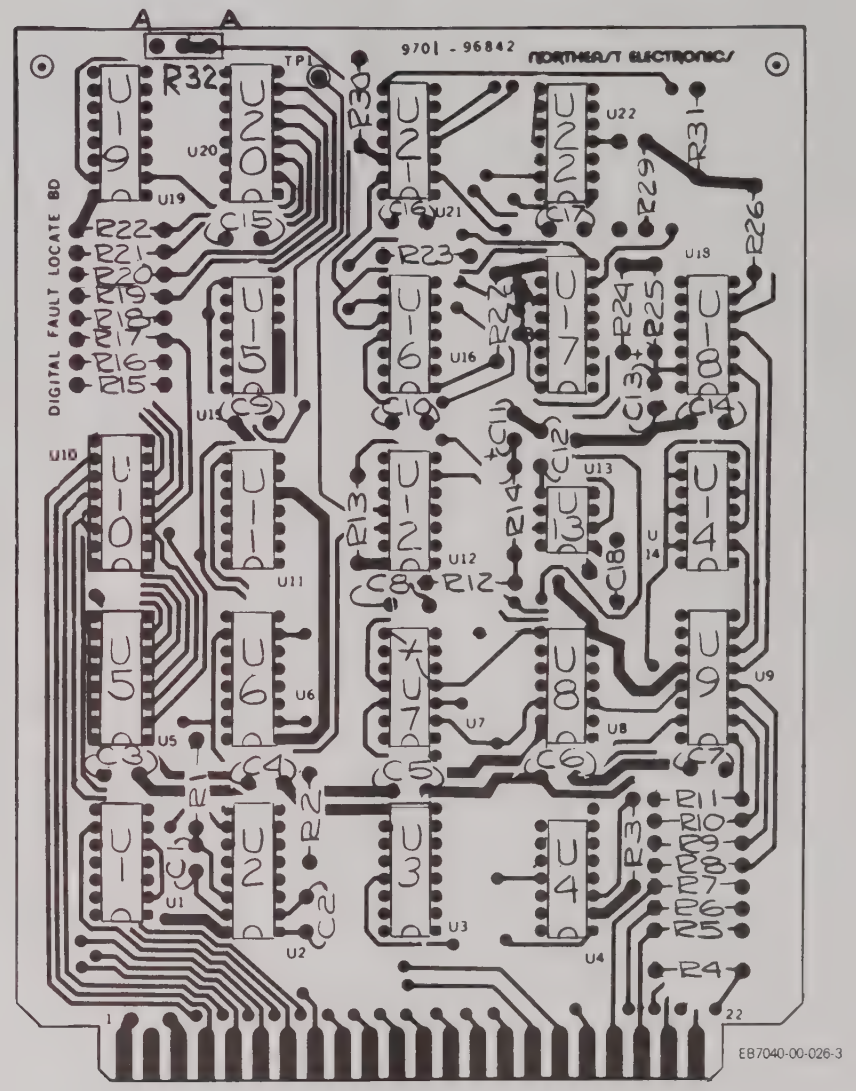


Figure 6—15. 7040 Digital Fault Locate Generator Assembly A8 Parts Location Diagram

ACTIVE LINE (LOW)	FAULT LOCATE FREQ (HZ)
FLS 1	839.1
FLS 2	927.9
FLS 3	1048.9
FLS 4	1206.3
FLS 5	1340.3
FLS 6	1507.8
FLS 7	1723.2
FLS 8	2010.4
FLS 9	2193.2
FLS 10	2412.5
FLS 11	2680.6
FLS 12	3015.6

IC	TYPE	VCC	GND
U1,7	74LS00	14	7
U2	96S02	16	8
U3,12	74LS74	14	7
U4,11	74LS93	5	10
U5,10	74S188	16	8
U6	74LS175	16	8
U8	74LS197	14	7
U9	7445	16	8
U13	NE555	8	1
U14,18	7405	14	7
U15	7410	14	7
U16	74LS27	14	7

IC	TYPE	VCC	GND
U17	74LS76	5	13
U19,20	74LS163	16	8
U21,22	74LS12	14	7

HIGHEST REFERENCE DESIGNATIONS			
C18	R31	U22	

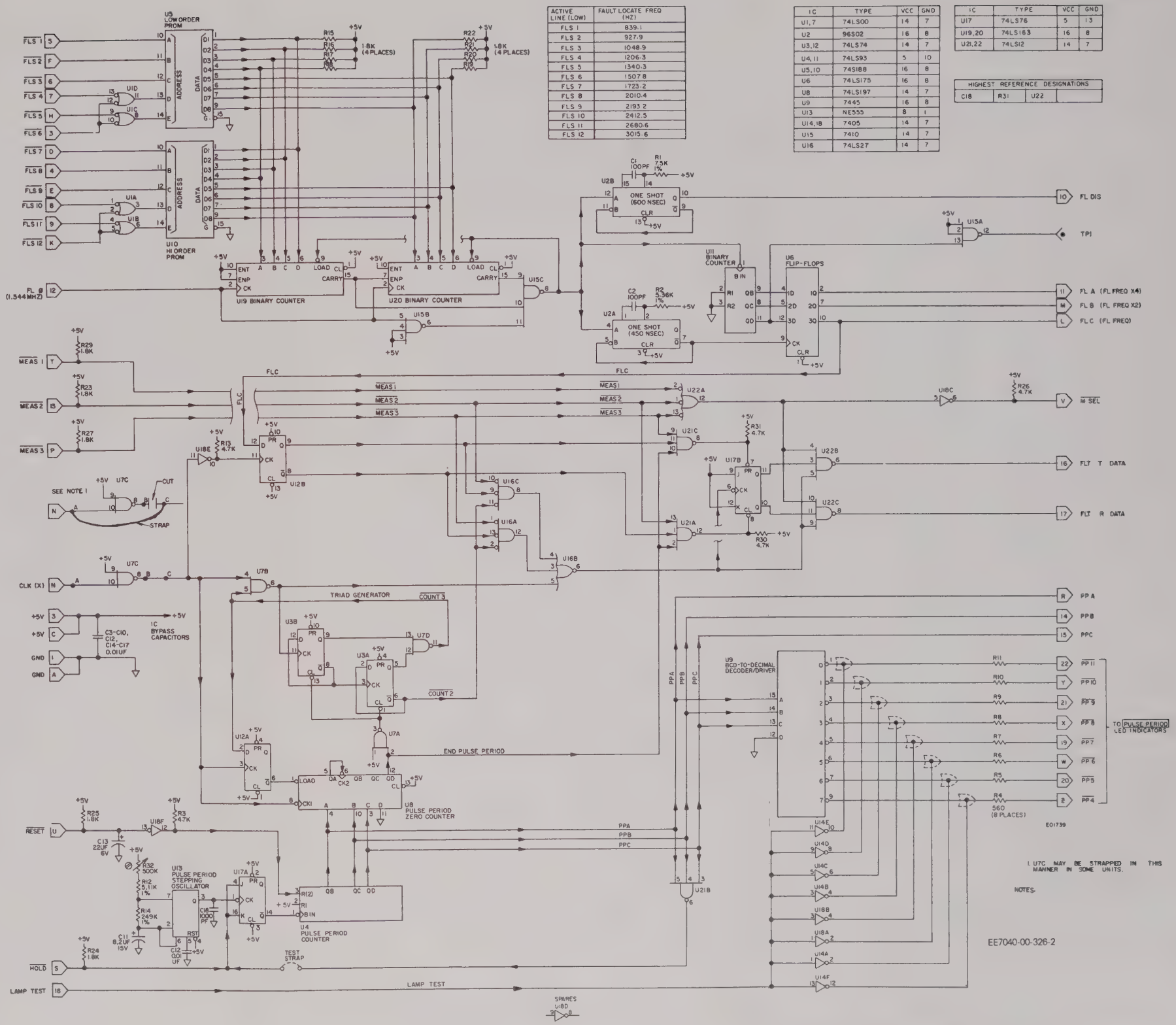


Figure 6—16. 7040 Digital Fault Locate Generator Assembly A8 Schematic Diagram

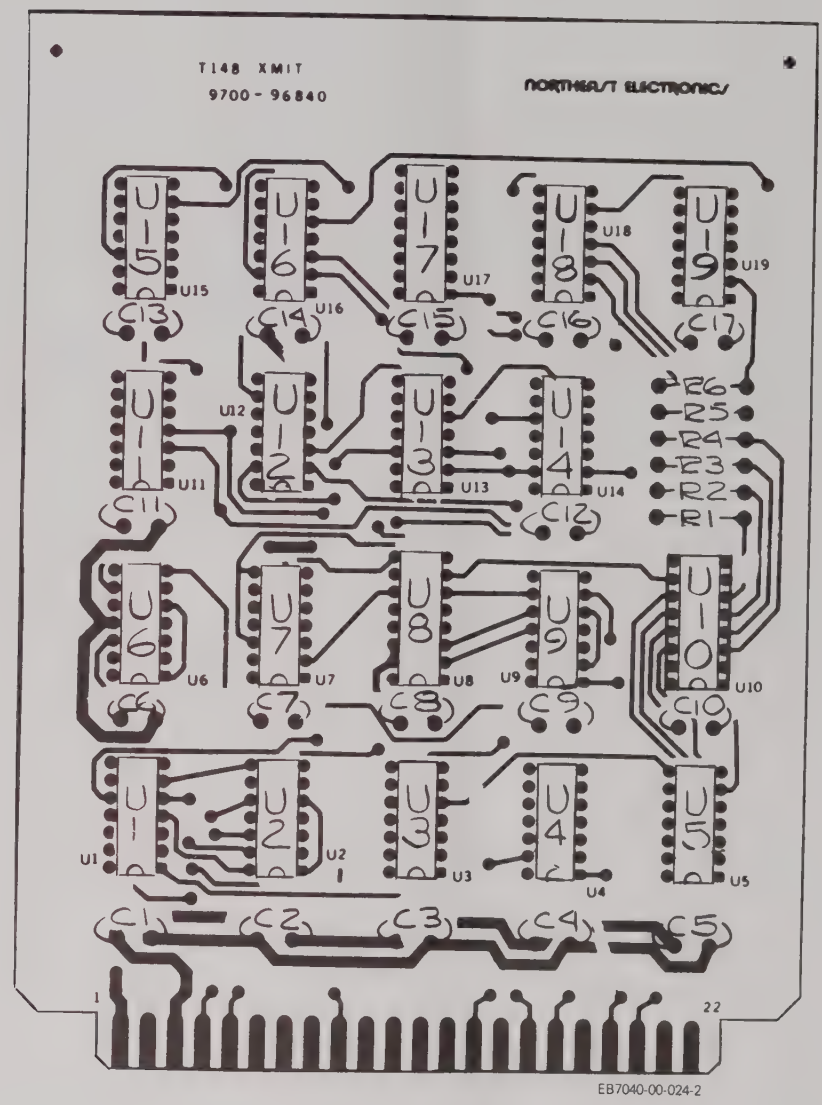


Figure 6—17. 7040 T148 Generator Assembly A6 Parts Location Diagram

IC	TYPE	VCC	GND
U1, U14	74LS02	14	7
U2, U6	74LS73	4	11
U3, U7, U12, U16	74LS74	14	7
U4	74LS04	14	7
U5	74LS164	14	7
U8	74LS193	16	8
U9	74LS27	14	7
U10	74LS188	16	8
U11	74LS10	14	7
U13, U15	74LS00	14	7
U17	74LS161	16	8
U18, U19	74LS95	14	7

NOTE:
1. ALL IC'S BYPASSED WITH 0.01UF
2. THE STRAPPING METHOD SHOWN MAY BE APPLIED ON SOME UNITS.

	+1	0	-1
T148 T DATA	L	H	H
T148 R DATA	H	H	L

SPARES: U4B, U4C, U4D, U4E, U11A

HIGHEST REFERENCE DESIGNATIONS			
C17	R5	U19	

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Figure 6—18. 7040 T148 Generator Assembly A6 Schematic Diagram

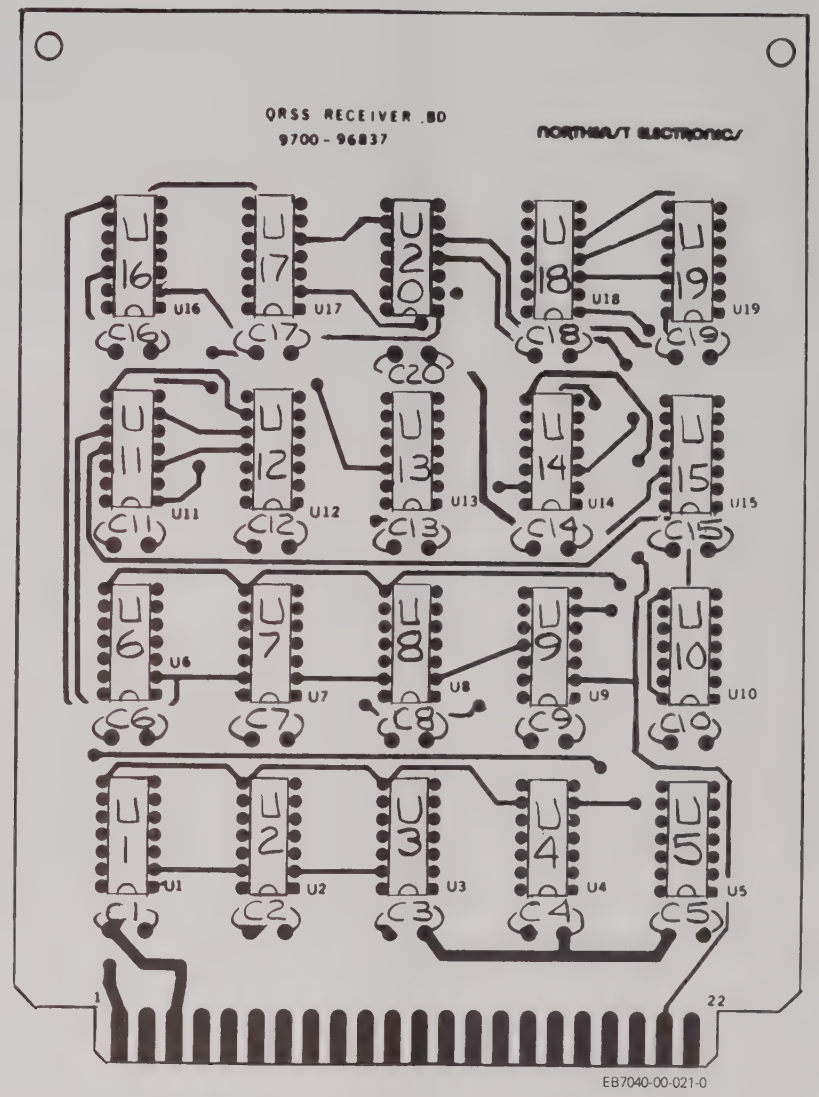
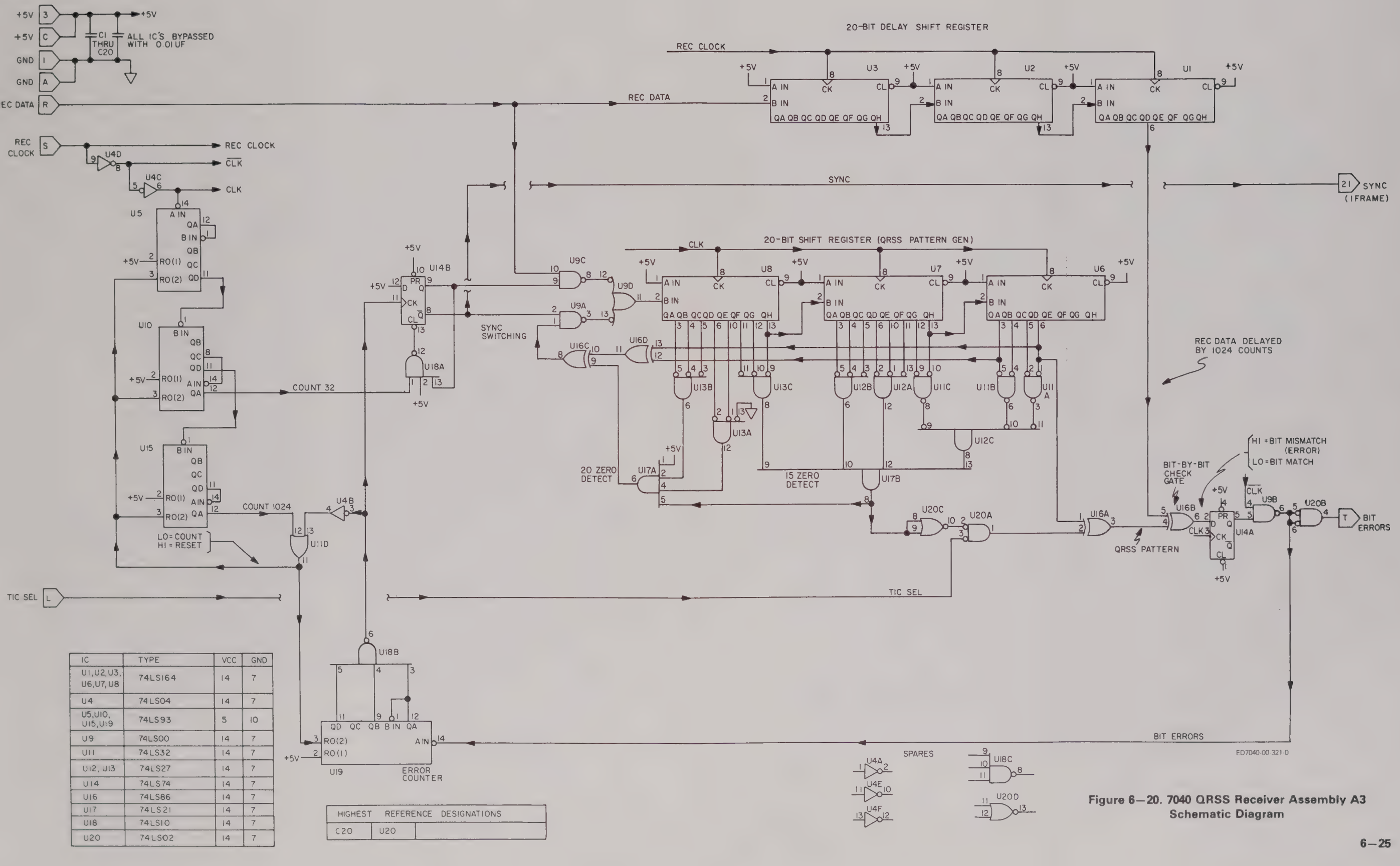


Figure 6—19. 7040 QRSS Receiver Assembly A3 Parts Location Diagram



IC	TYPE	VCC	GND
U1, U2, U3, U6, U7, U8	74LS164	14	7
U4	74LS04	14	7
U5, U10, U15, U19	74LS93	5	10
U9	74LS00	14	7
U11	74LS32	14	7
U12, U13	74LS27	14	7
U14	74LS74	14	7
U16	74LS86	14	7
U17	74LS21	14	7
U18	74LS10	14	7
U20	74LS02	14	7

HIGHEST REFERENCE DESIGNATIONS		
C20	U20	

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Figure 6—20. 7040 QRSS Receiver Assembly A3 Schematic Diagram

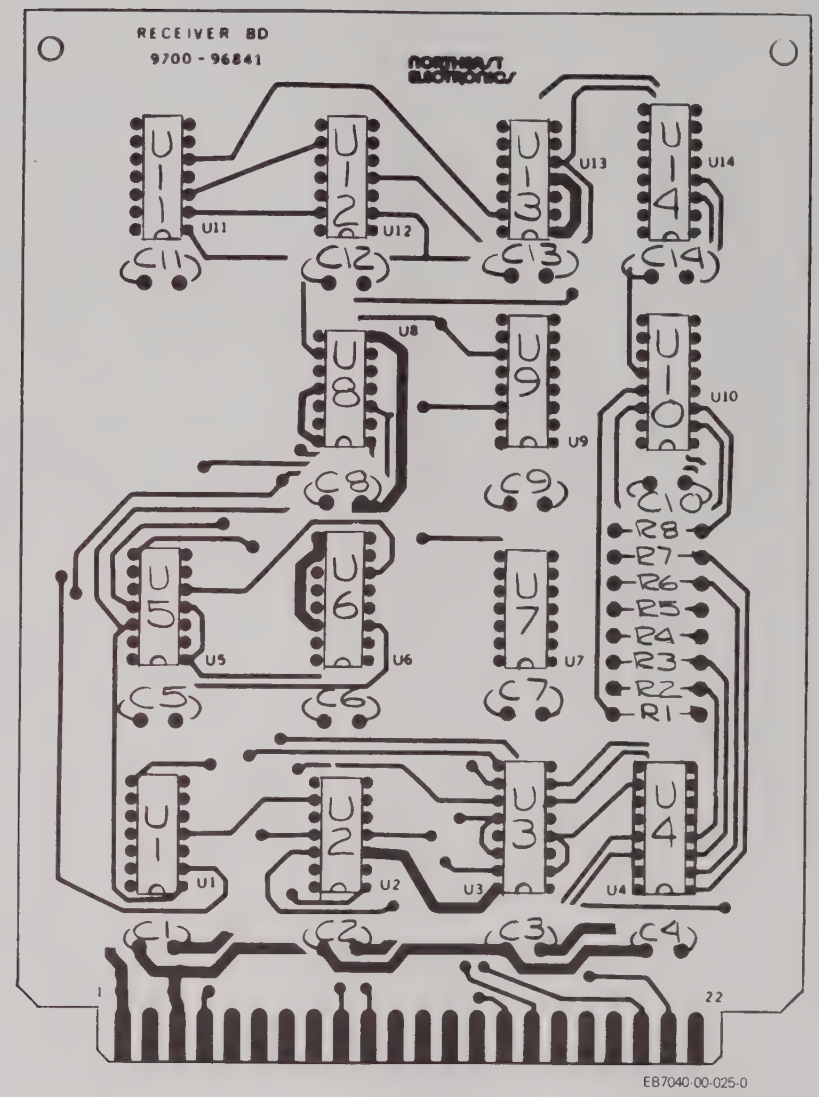
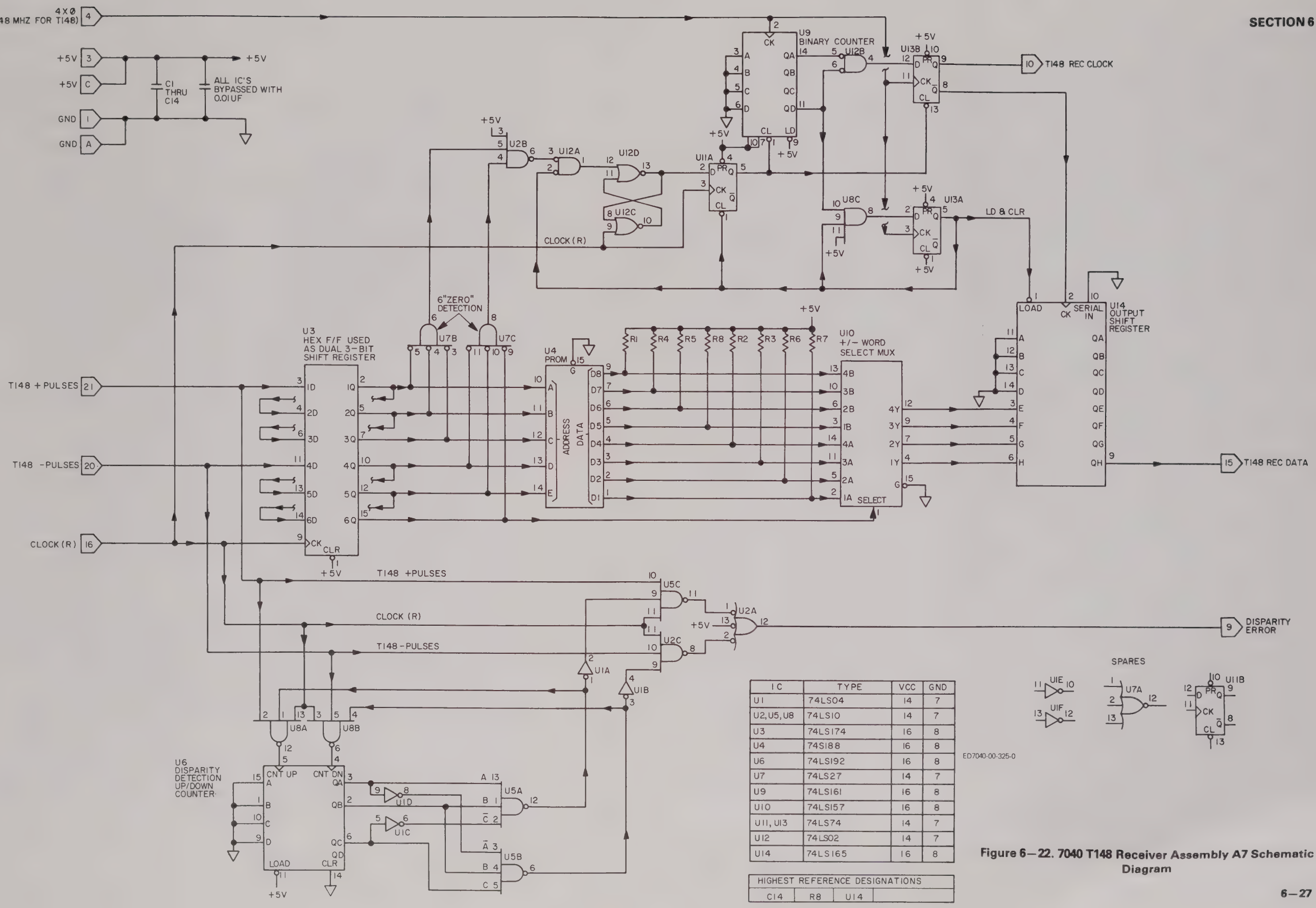


Figure 6—21. 7040 T148 Receiver Assembly A7 Parts Location Diagram



IC	TYPE	VCC	GND
U1	74LS04	14	7
U2,U5,U8	74LS10	14	7
U3	74LS174	16	8
U4	74S188	16	8
U6	74LS192	16	8
U7	74LS27	14	7
U9	74LS161	16	8
U10	74LS157	16	8
U11, U13	74LS74	14	7
U12	74LS02	14	7
U14	74LS165	16	8

HIGHEST REFERENCE DESIGNATIONS			
C14	R8	U14	

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Figure 6—22. 7040 T148 Receiver Assembly A7 Schematic Diagram

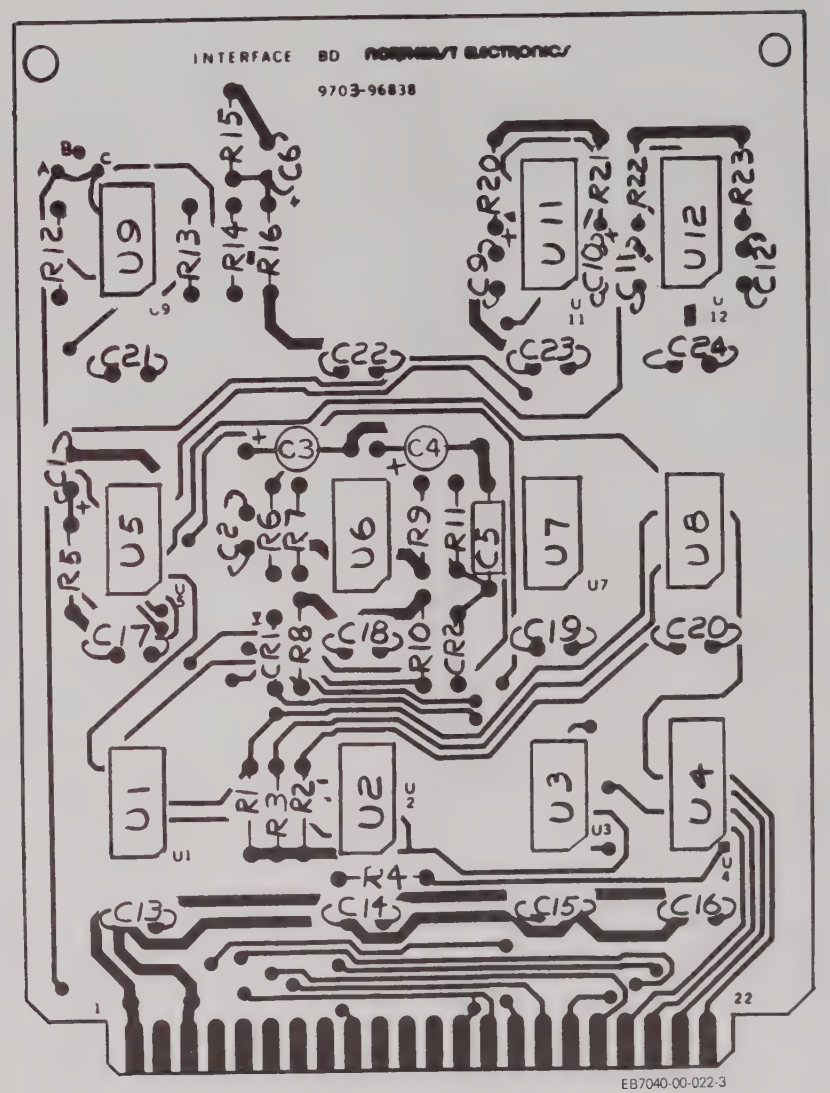
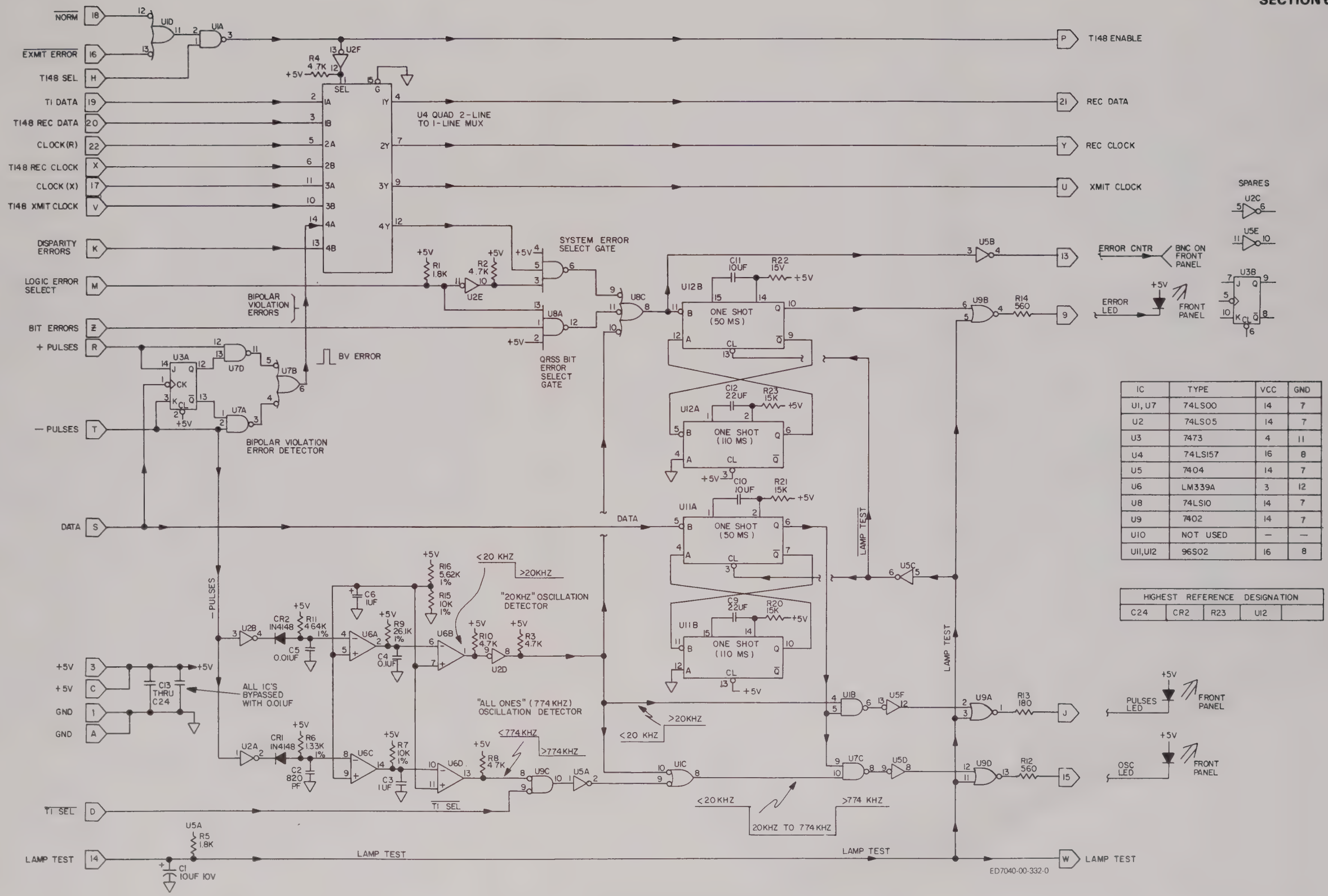


Figure 6—23. 7040 Interface Assembly A4 Parts Location Diagram



IC	TYPE	VCC	GND
U1, U7	74LS00	14	7
U2	74LS05	14	7
U3	7473	4	11
U4	74LS157	16	8
U5	7404	14	7
U6	LM339A	3	12
U8	74LS10	14	7
U9	7402	14	7
U10	NOT USED	—	—
U11,U12	96S02	16	8

HIGHEST REFERENCE DESIGNATION				
C24	CR2	R23	U12	

Figure 6—24. 7040 Interface Assembly A4 Schematic Diagram

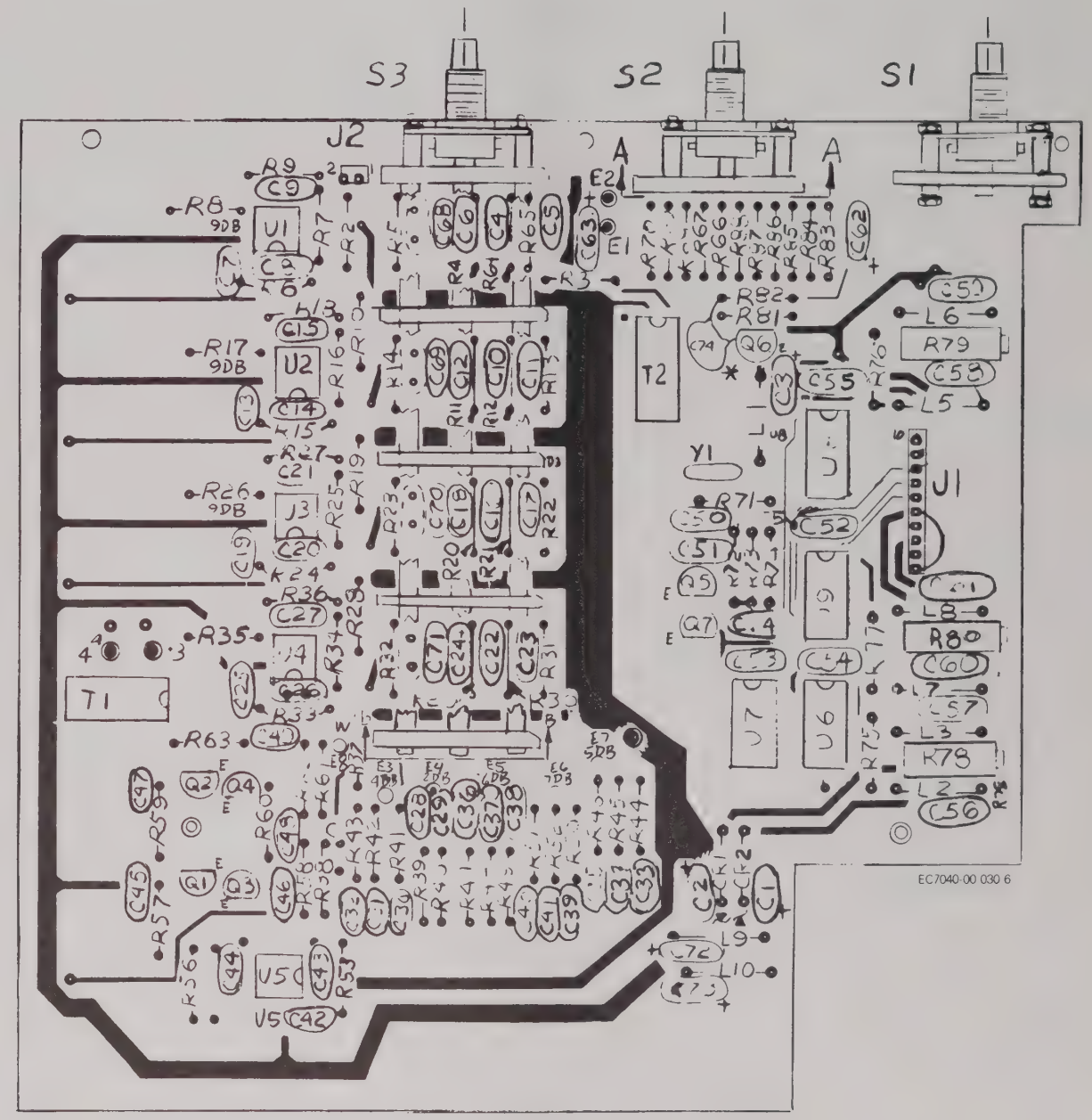
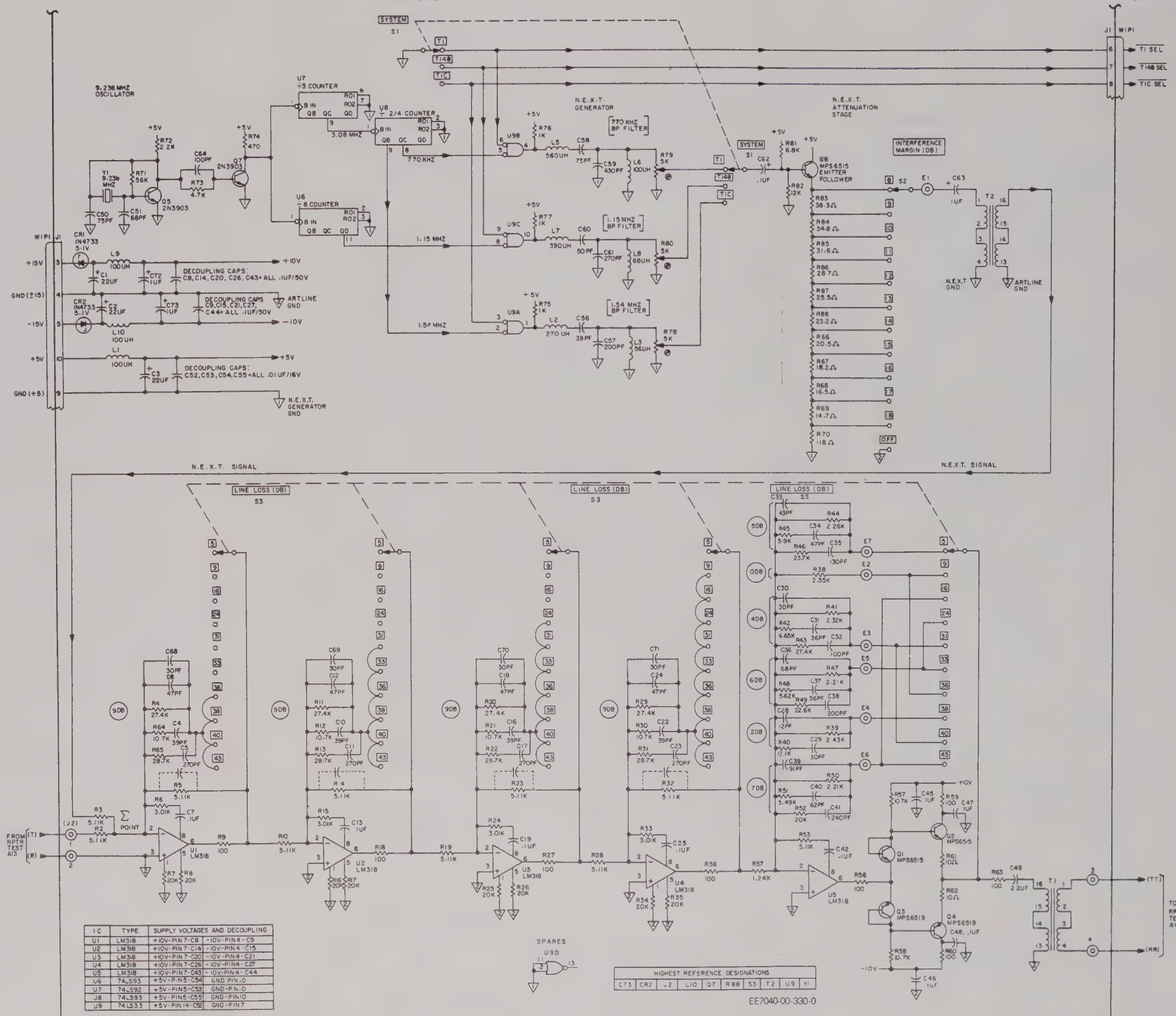


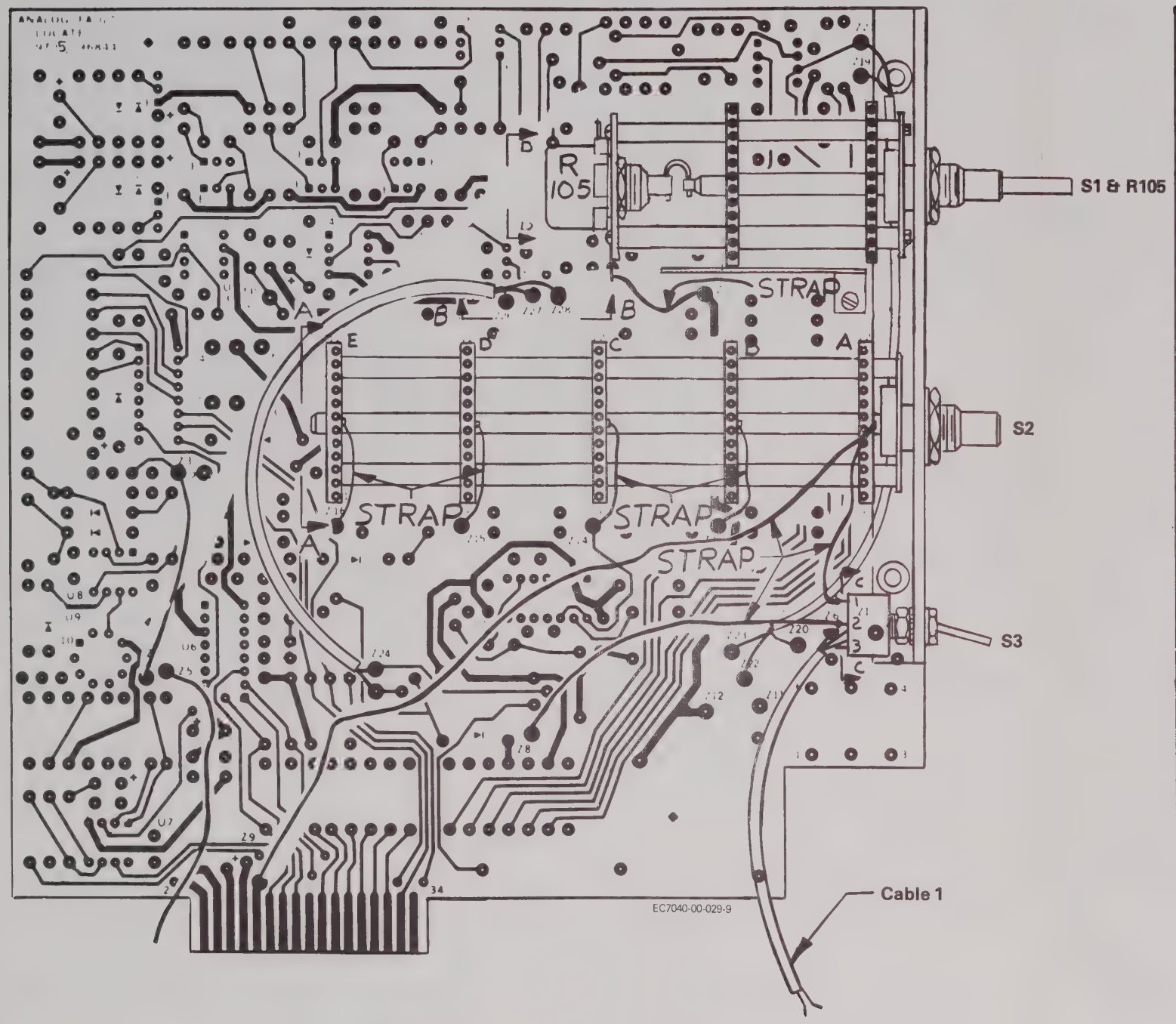
Figure 6—25. 7040 Artline Assembly A11 Parts Location Diagram



IC	TYPE	SUPPLY VOLTAGES AND DECOUPLING
U1	LM318	+10V-PIN 7-C8 | -10V-PIN 4-C9
U2	LM318	+10V-PIN 7-C14 | -10V-PIN 4-C15
U3	LM318	+10V-PIN 7-C20 | -10V-PIN 4-C21
U4	LM318	+10V-PIN 7-C26 | -10V-PIN 4-C27
U5	LM318	+10V-PIN 7-C43 | -10V-PIN 4-C44
U6	74LS93	+5V-PIN 5-C54 | GND-PIN 0
U7	74LS92	+5V-PIN 5-C53 | GND-PIN 0
U8	74LS93	+5V-PIN 5-C55 | GND-PIN 10
U9	74LS33	+5V-PIN 14-C52 | GND-PIN 7

HIGHEST REFERENCE DESIGNATIONS								
C73	CR2	J2	L10	Q7	R88	S3	T2	U9	Y1

Figure 6—26. 7040 Artline Assembly A11 Schematic Diagram



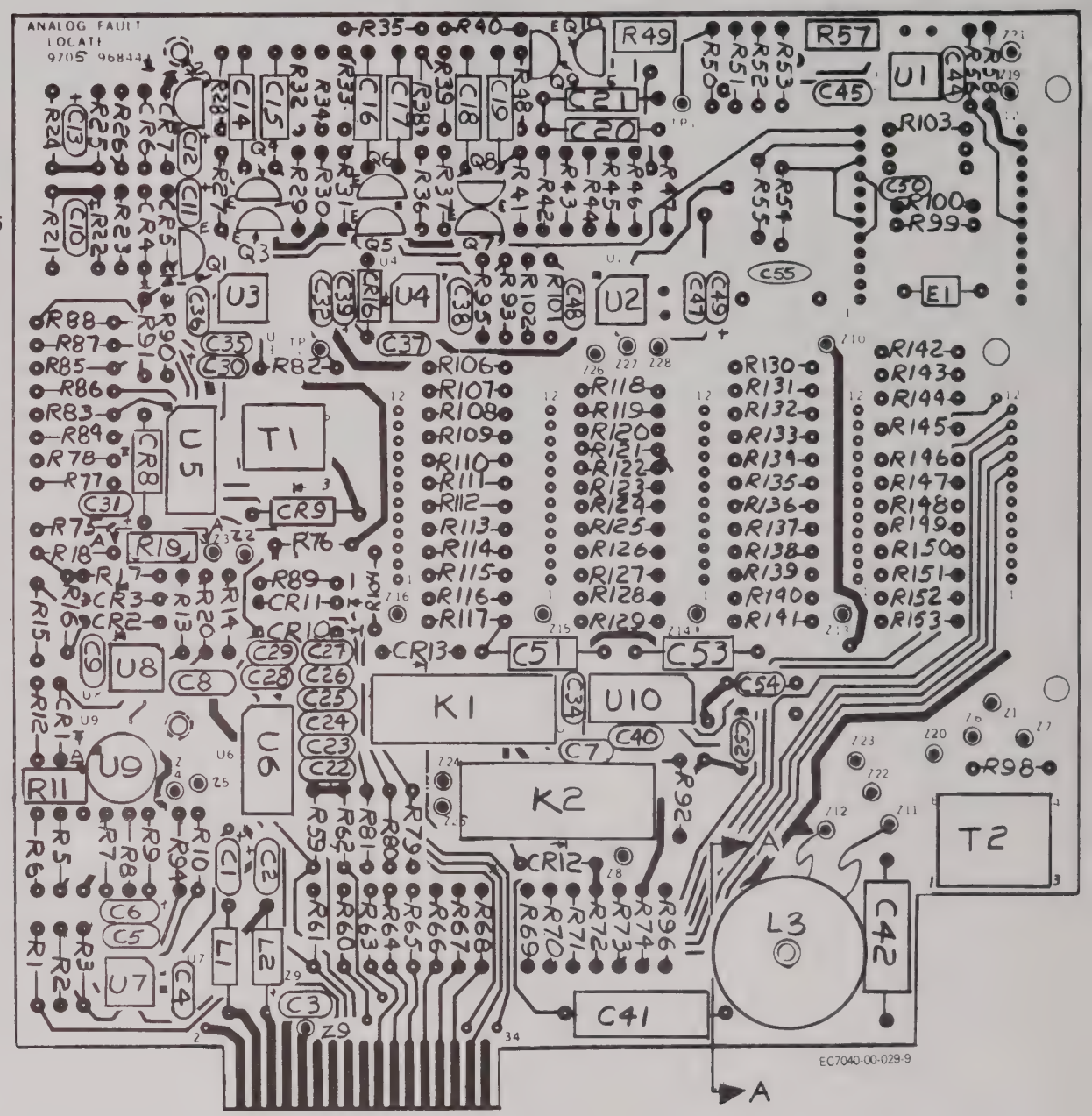


Figure 6—27. 7040 Analog Fault Locate Assembly A10
Parts Location Diagram

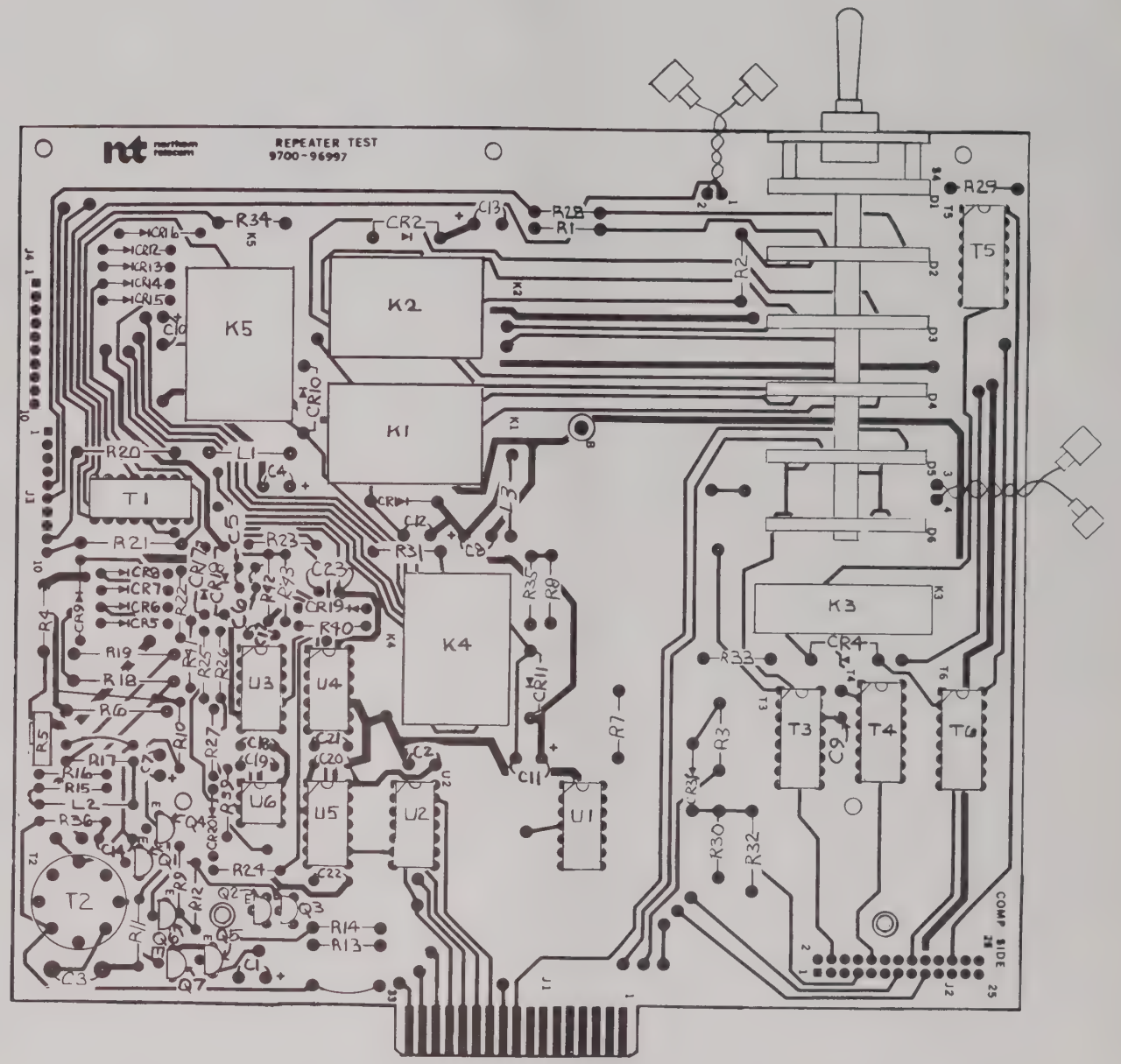
SI-B POSITION	ATTEN (DB)
-90	0.1
-80	10.1
-70	20.1
-60	30.1
-50	40.1
-40	10.1
-30	20.1
-20	30.1
-10	40.1
0 CAL	50.1

PULSE PERIOD	LOG LEVEL PPC	PPB	PPA	U3 GAIN (DB)
11	0	0	0	34.96
10	0	0	1	34.15
9	0	1	0	33.22
8	0	1	1	32.19
7	1	0	0	30.88
6	1	0	1	29.87
5	1	1	0	27.86
4	1	1	1	26.48

IC	TYPE	SUPPLY VOLTAGES	
U1, 2, 3	LM741CN	+15V(PIN 7)	-15V(PIN4)
U4,7,8	LM1458	+15V(PIN8)	-15V(PIN 4)
U5,6	CD4051	+ 7.5V(PIN16)	-7.5V(PIN7)
U9	CA3019	—	—
U10	RC 4136	+15V(PIN11)	-15V(PIN7)

HIGHEST REFERENCE DESIGNATION					
C55	CR16	E1	K2	L3	Q10
R153	S3	T2	U10		

Figure 6—28. Analog Fault Locate Assembly A10 Schematic Diagram



EC7040-00-027-0

Figure 6—29. 7040 Repeater Test Assembly A13 Parts Location Diagram

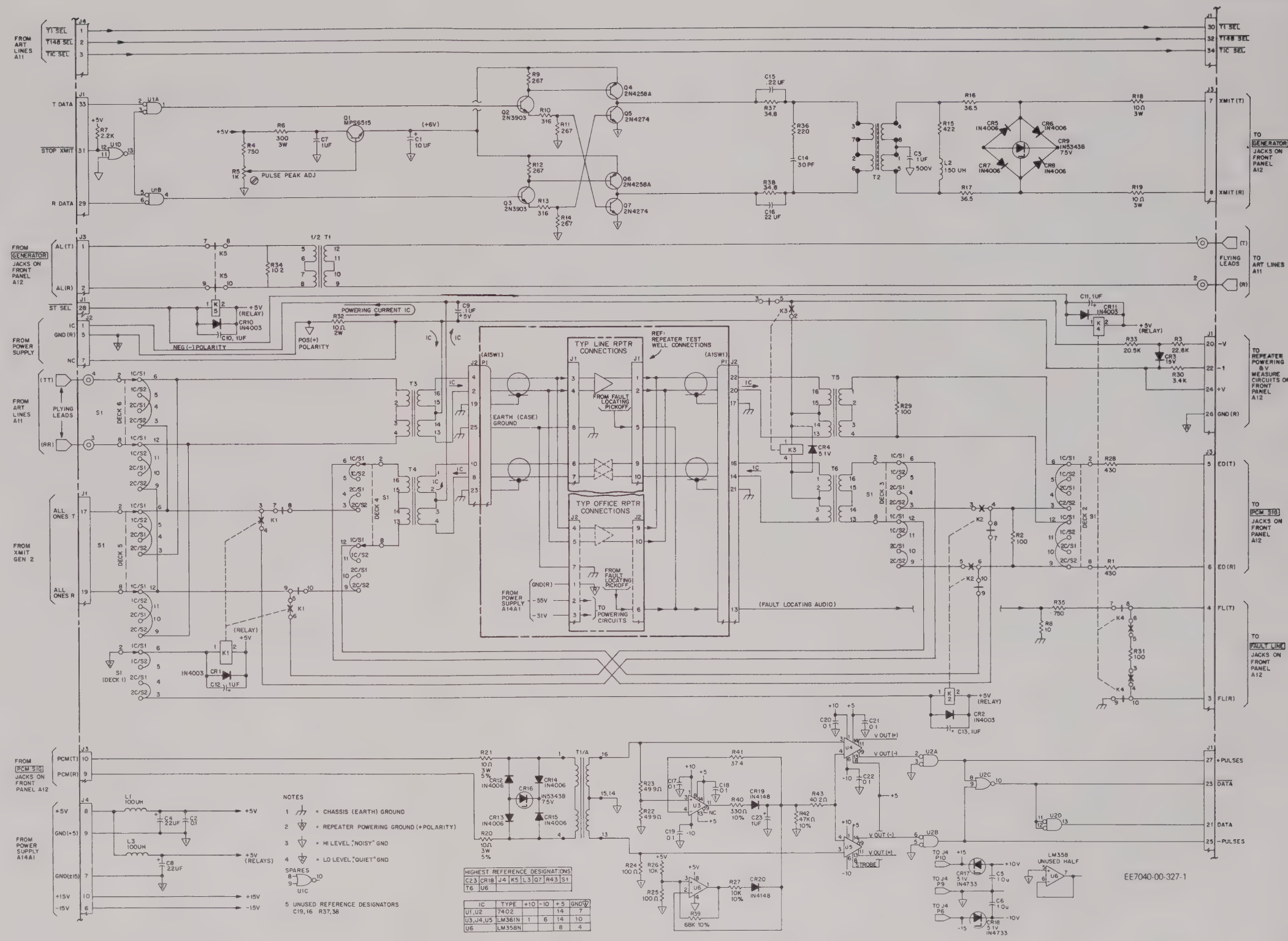
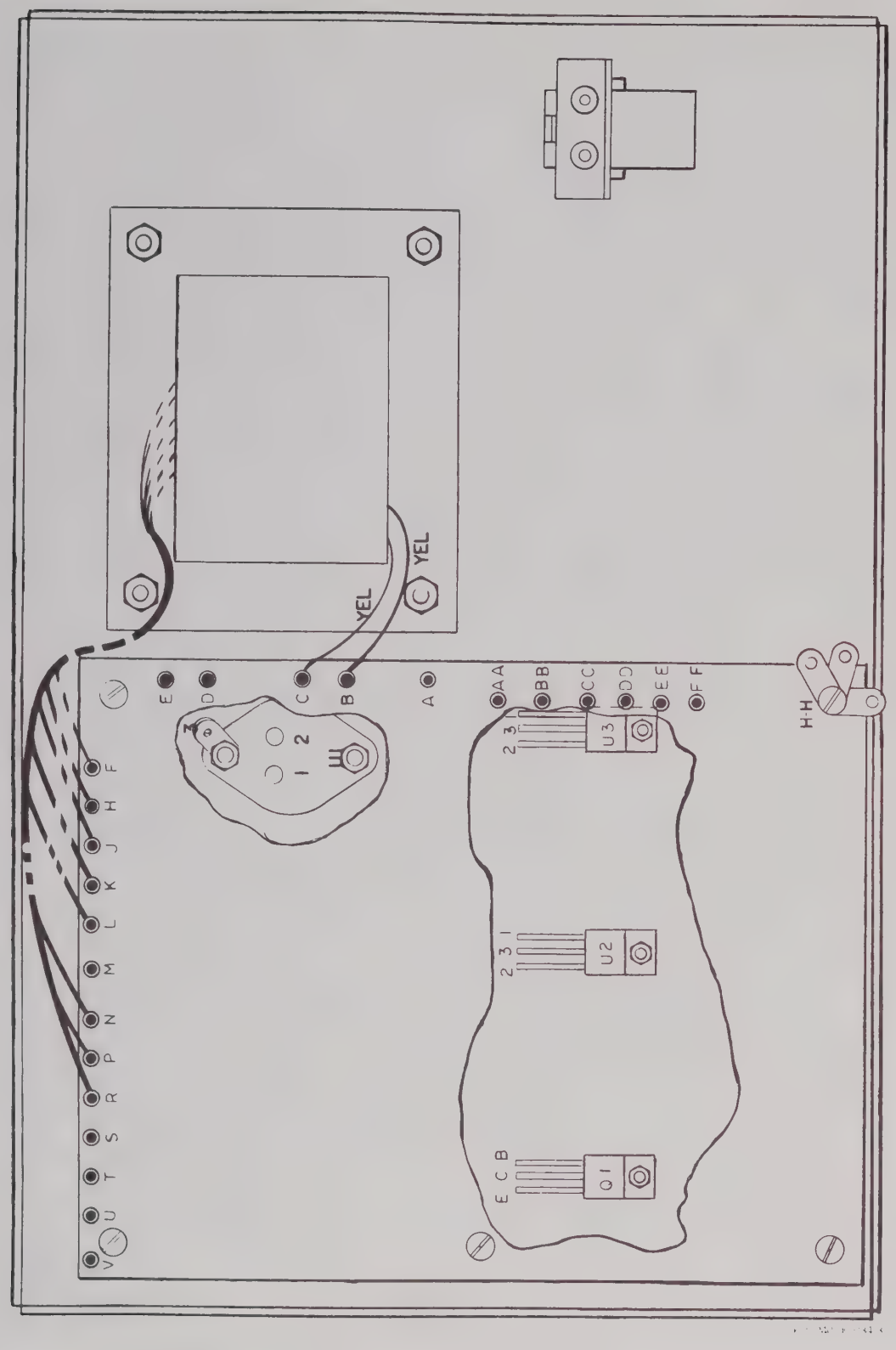
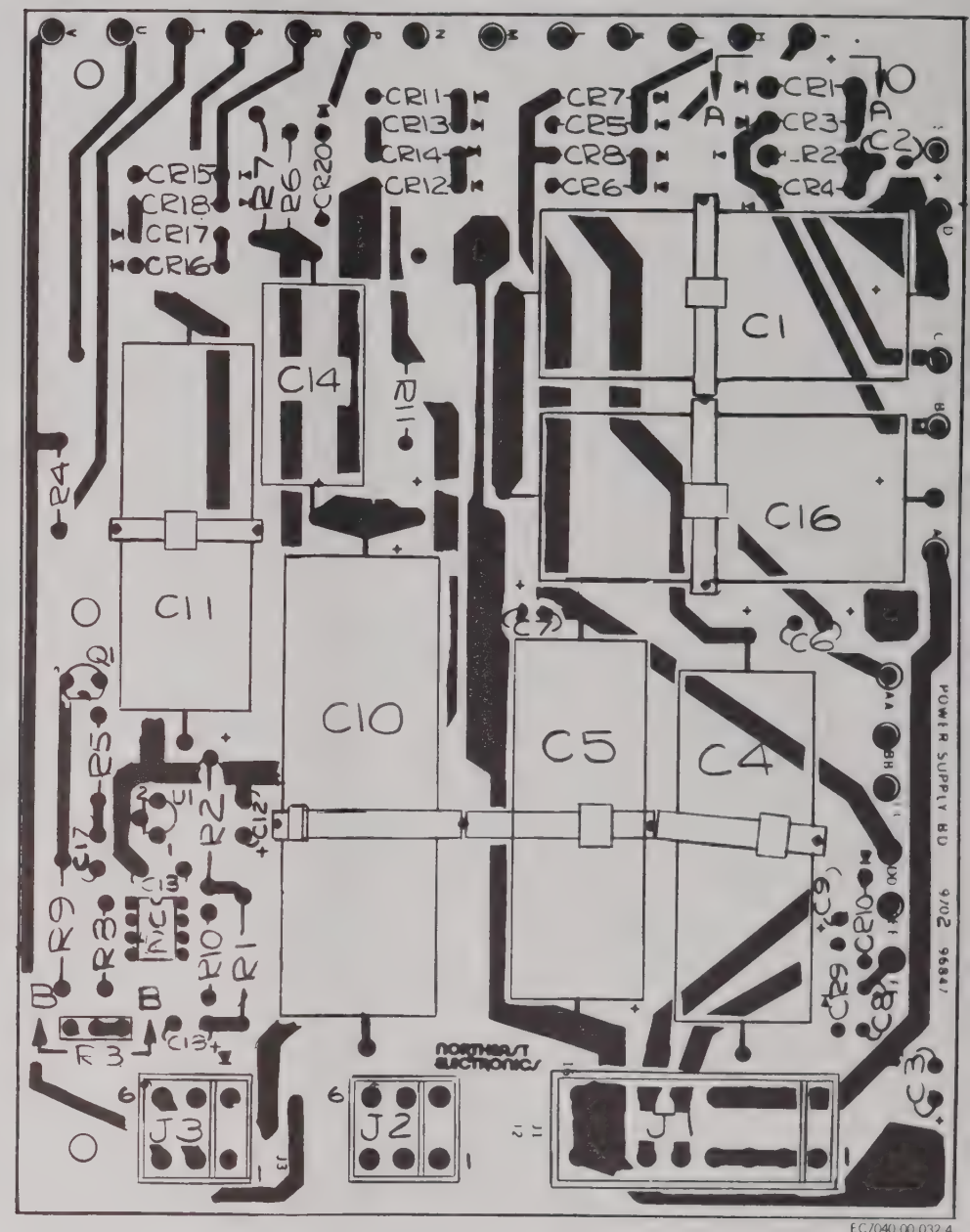


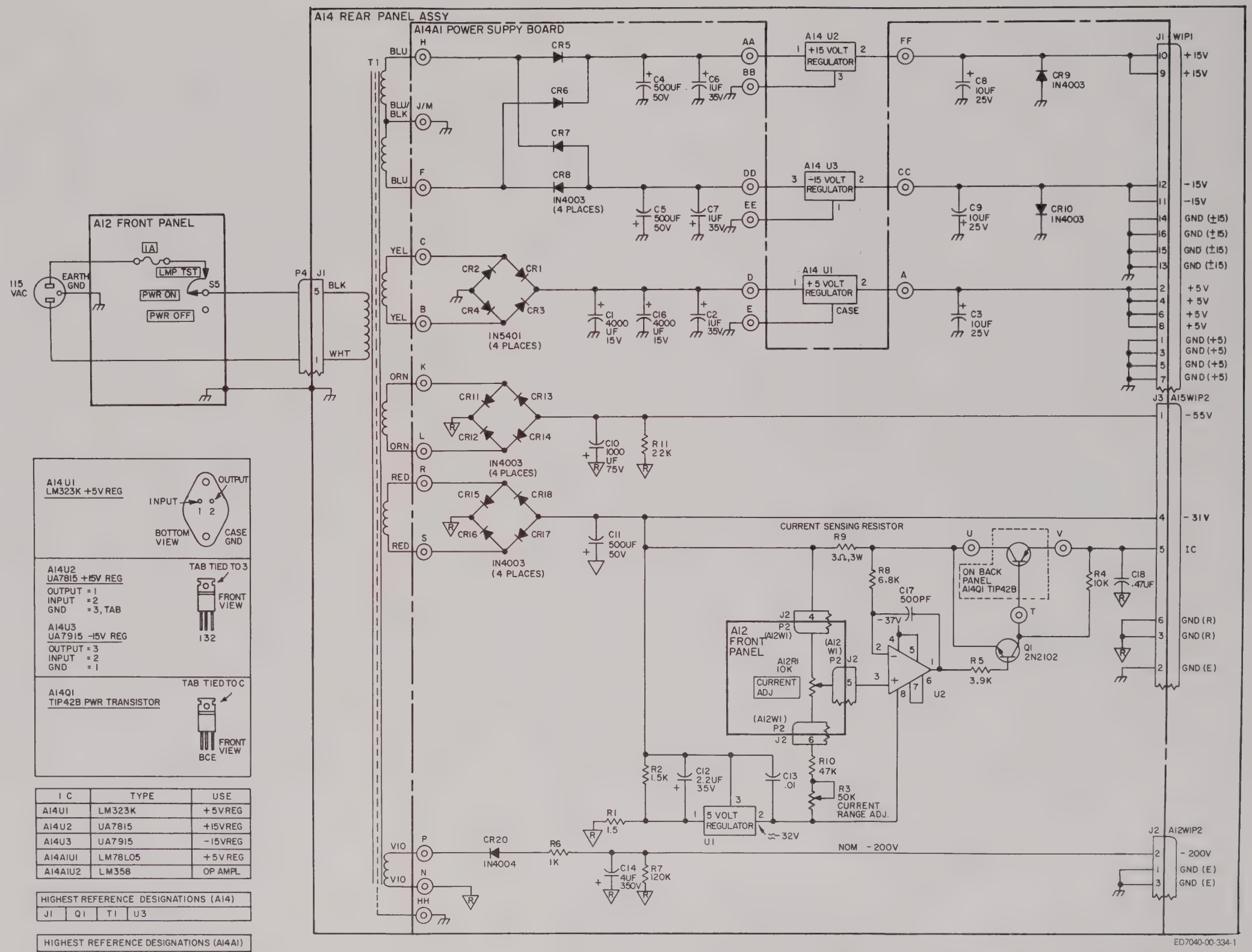
Figure 6—30. 7040 Repeater Test Assembly A13 Schematic Diagram





EC7040-00-032-4

Figure 6—31. 7040 Power Supply Assembly A14 Parts Location Diagram

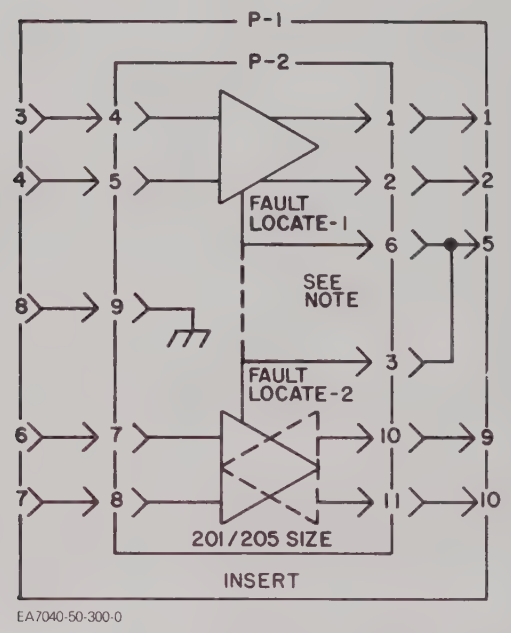


I C	TYPE	USE
A14U1	LM323K	+5VREG
A14U2	UA7815	+15VREG
A14U3	UA7915	-15VREG
A14A1U1	LM78L05	+5VREG
A14A1U2	LM358	OP AMPL

HIGHEST REFERENCE DESIGNATIONS (A14)			
J1	Q1	T1	U3

HIGHEST REFERENCE DESIGNATIONS (A14A1)					
C17	CR20	J3	Q1	R11	U2

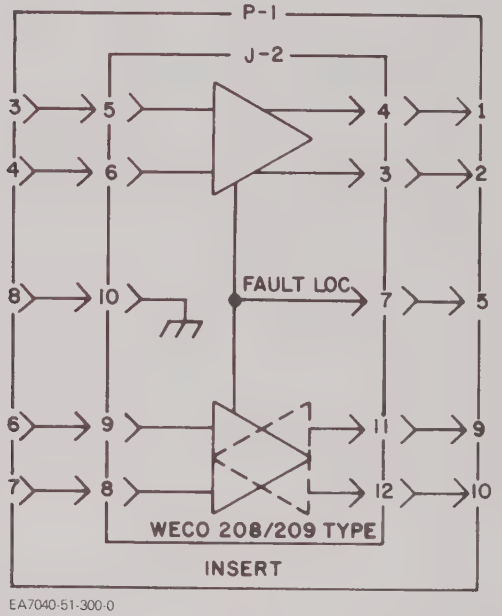
Figure 6–32. 7040 Power Supply Assembly A14 Schematic Diagram



NOTES:

1. DEPENDING UPON MANUFACTURER, PIN 3 OF REPEATER MAYBE EITHER FAULT LOCATE OUTPUT 2, EARTH GROUND OR OPEN.
2. TI OR TI-C LINE REPEATER MFGRS:
   GTE-LENKURT TI-C MANY TI

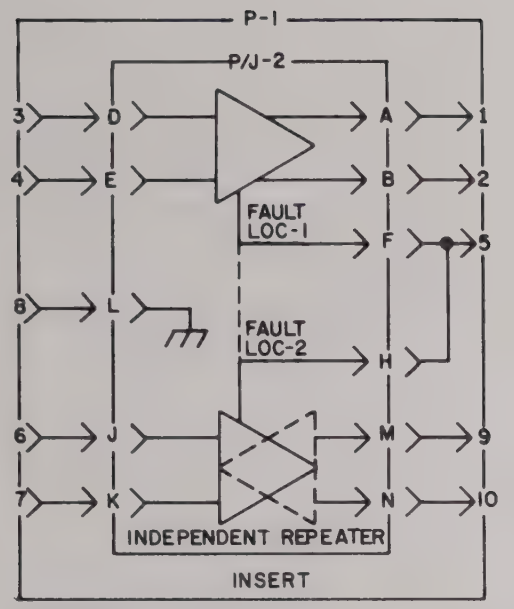
Figure 6—33. 7040-50 Repeater Insert Schematic Diagram



NOTE:

TI MINATURIZED LINE REPEATERS
MFGRS: WECO
GE/WESCOM
LYNCH 303
OTHERS

Figure 6—34. 7040-51 Repeater Insert Schematic Diagram

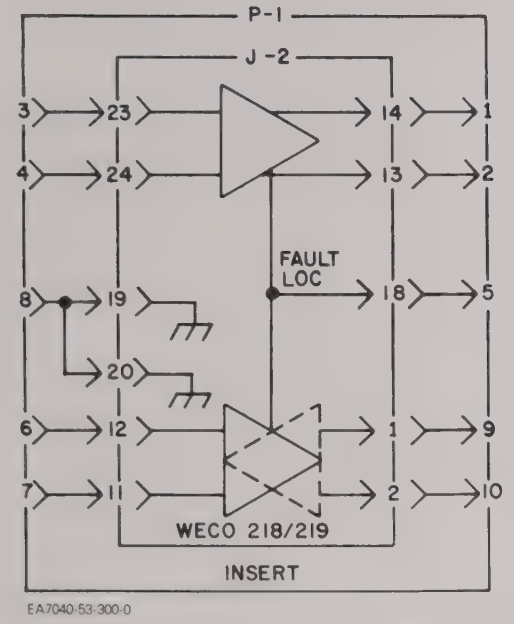


EA7040-52-300-0

MFGRS:

T1-ITT
STROMBERG-CARLSON
GTE-LENKURT
VICOM
AND OTHERS
T148-ITT

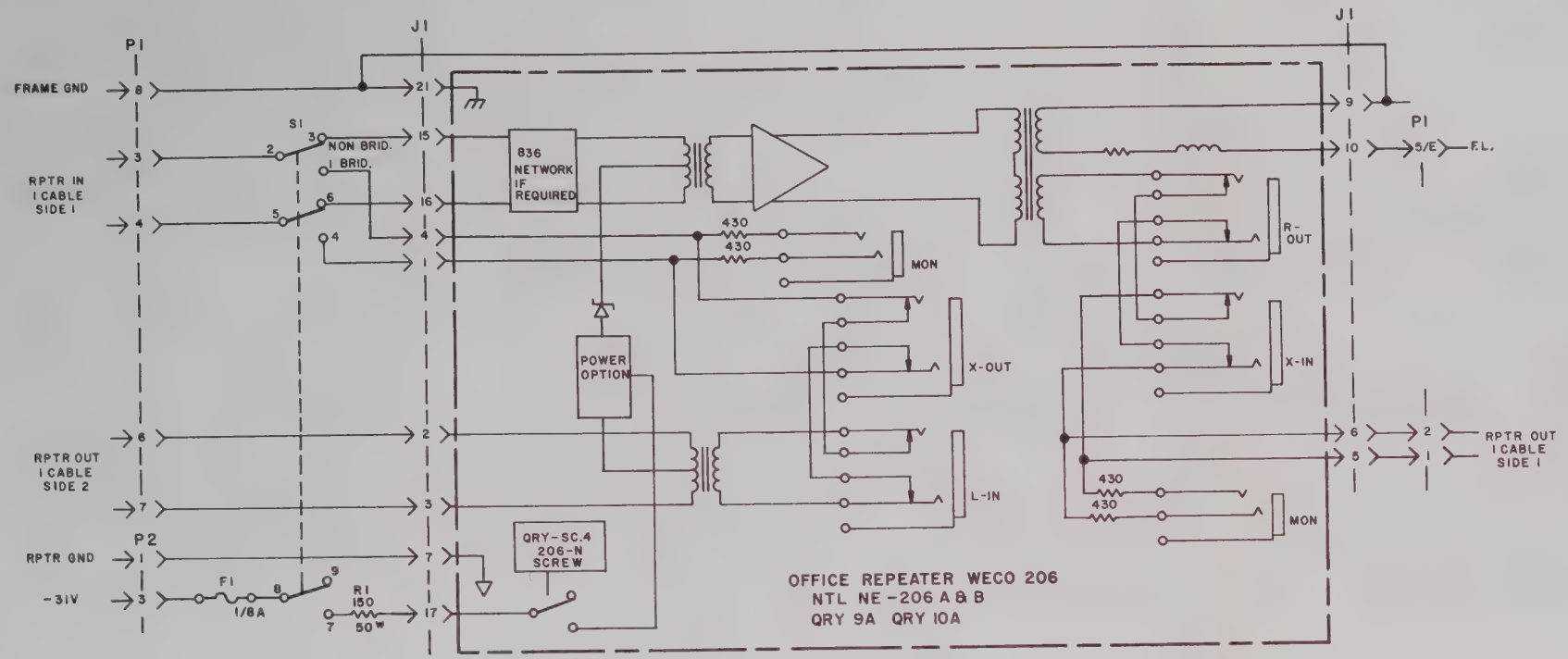
Figure 6—35. 7040-52 Repeater Insert Schematic Diagram



EA7040-53-300-0

NOTE:
T1-C 2 CABLE LINE REPEATER ONLY

Figure 6—36. 7040-53 Repeater Insert Schematic Diagram



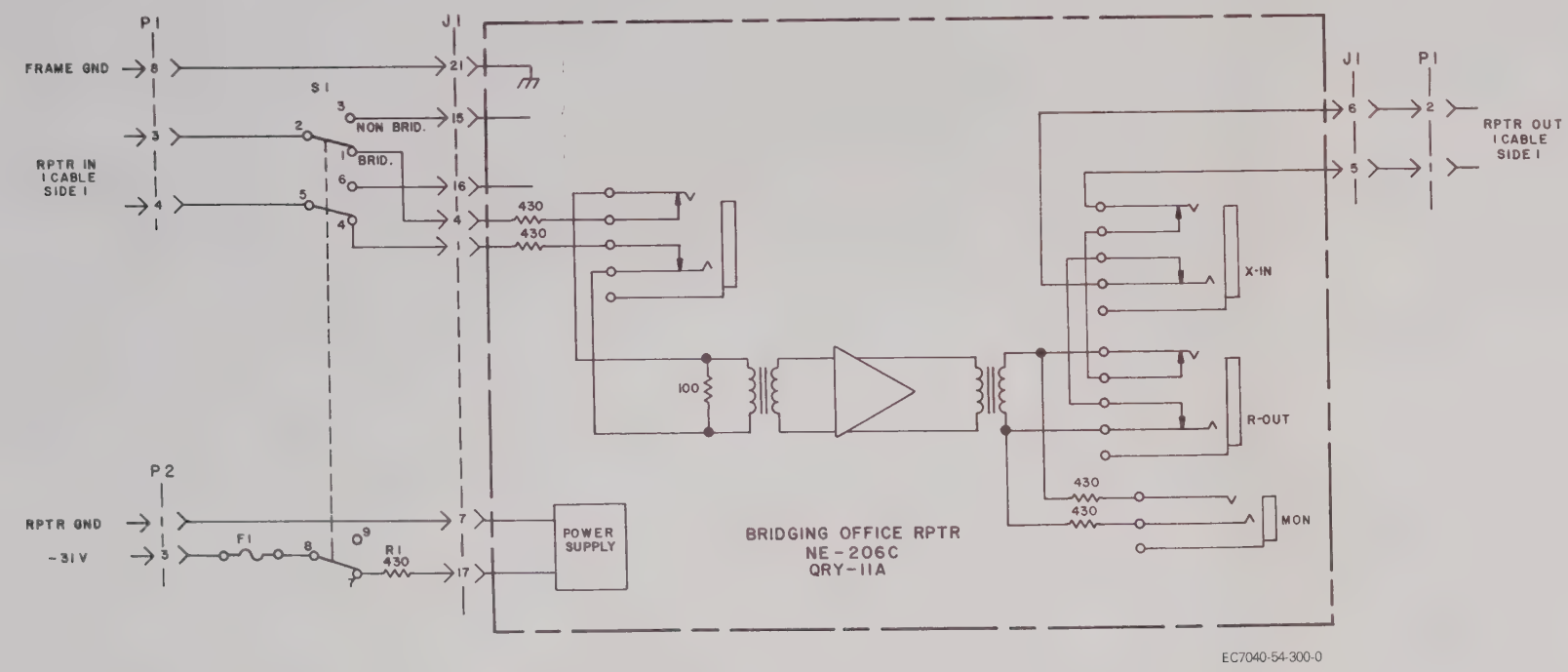


Figure 6—37. 7040-54 Repeater Insert Schematic Diagram

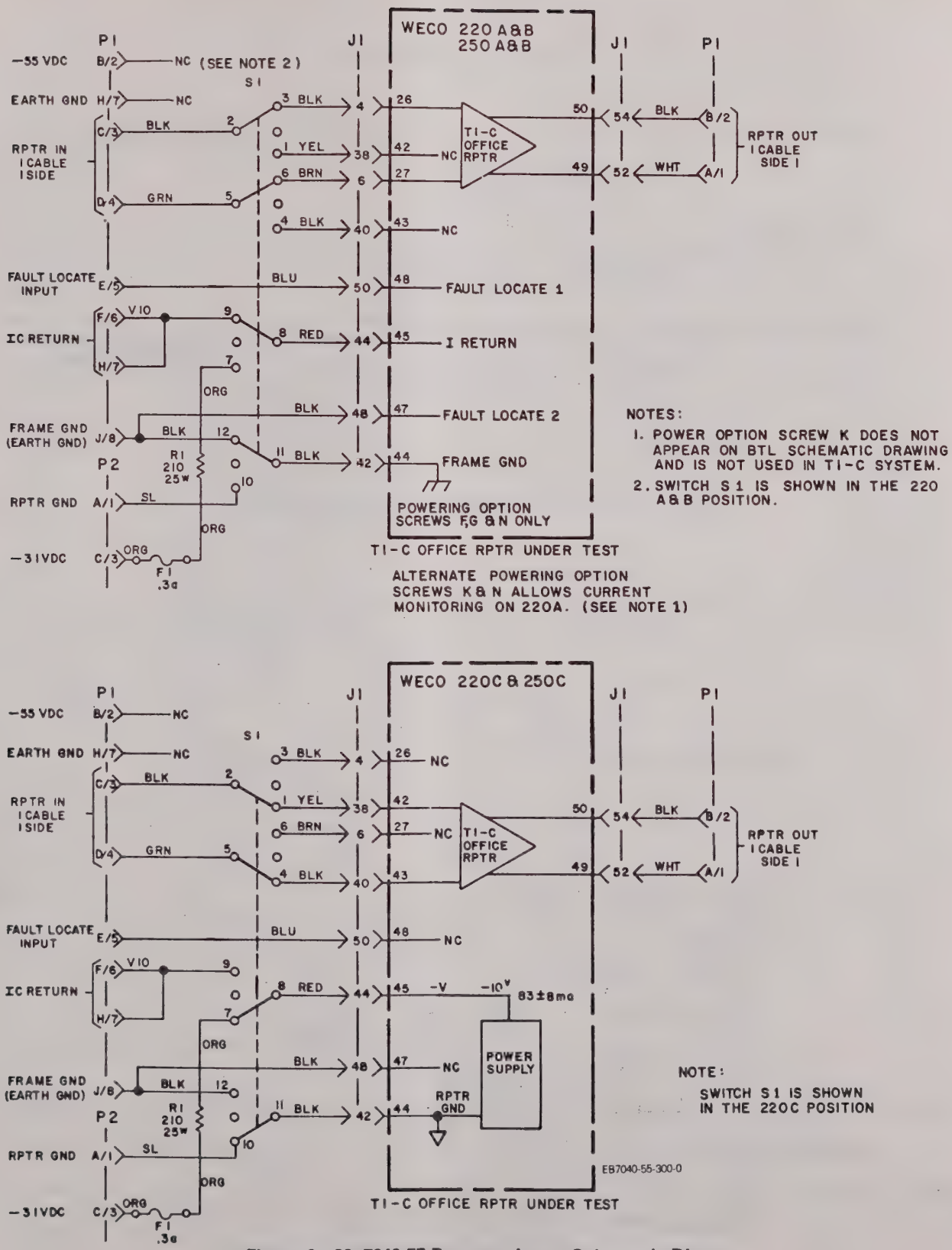
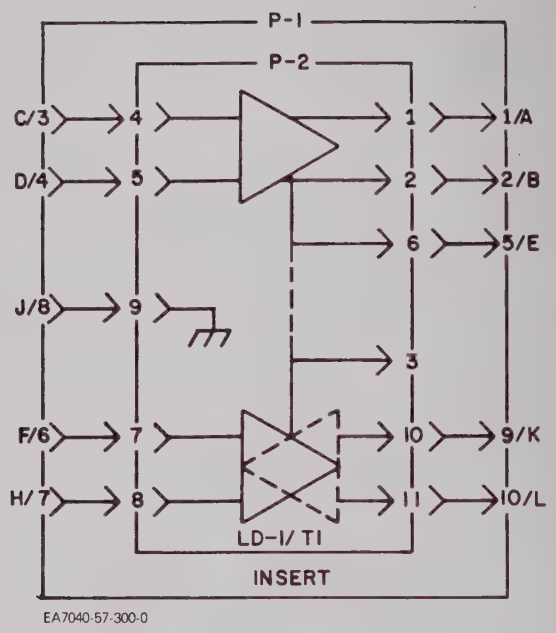


Figure 6—38. 7040-55 Repeater Insert Schematic Diagram



MFGR:
NORTHERN ELECTRIC NE-201/205 QA-B
QRY 4A&B/QRY5A&B

Figure 6—39. 7040-57 Repeater Insert Schematic Diagram

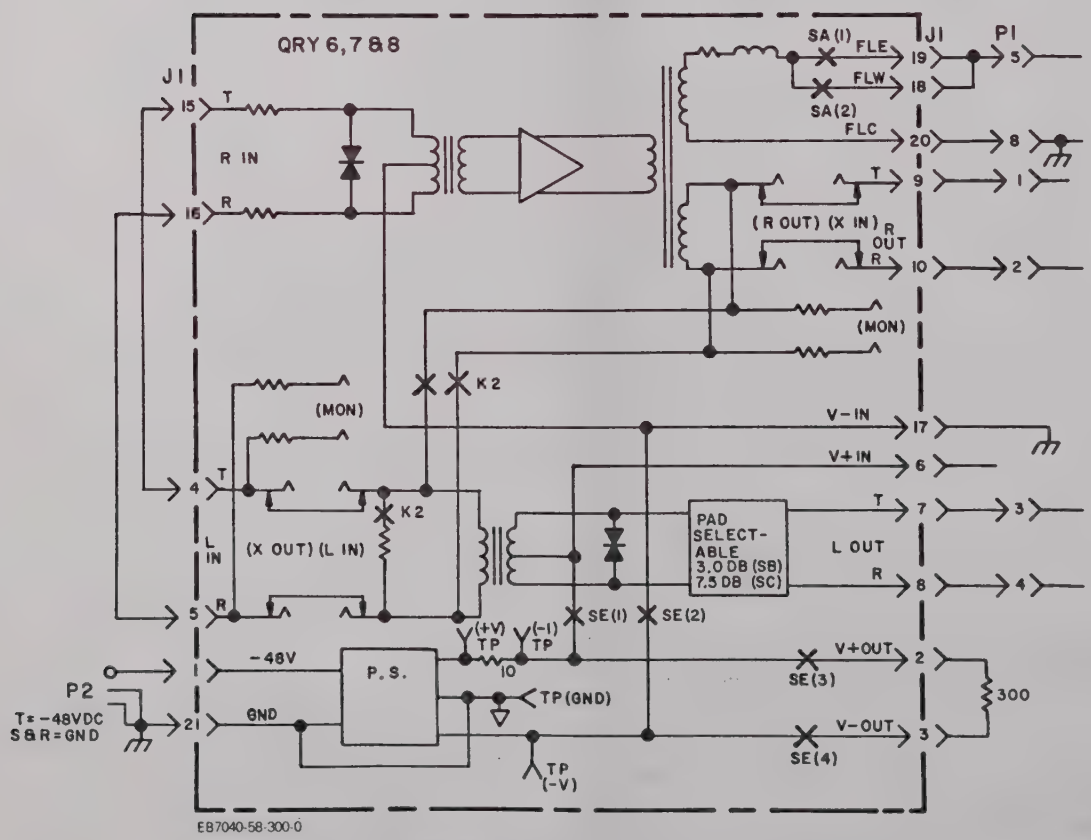


Figure 6—40. 7040-58 Repeater Insert Schematic Diagram

SECTION 7

ELECTRONIC PARTS LIST

7.1 This section contains the electronic parts list for all of the assemblies that comprise the Model 7040.

Table 7—1. 7040 Overall Parts List.

N O R T H E A S T REPLACABLE PARTS LIST FOR ASSEMBLY D7040-00-001
E L E C T R O N I C S O/A ASSY MODEL 7040 PAGE 1 REV 06 DATED 7/16/80

REFERENCE DESIGNATOR	D E S C R I P T I O N VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
A2	PC ASSY 96836 XMITT QRSS						A704000020
A3	PC ASSY 96837 QRSS REC.						A704000021
A4	PC ASSY 96838 INTERFACE						A704000022
A5	PC ASSY 96839 CLOCKS						A704000023
A6	PC ASSY 96840 T148 GEN						A704000024
A7	PC ASSY 96841 T148 REC						A704000025
A8	PC ASSY 96842 DIG FAULT						A704000026
A10	PC ASSY 96844 ANALOG						A704000029
A11	PC ASSY 96845 ART.LINE						A704000030
A12	FRONT PANEL ASSY						A704000033
A13	PC ASSY 96997 R@TR TEST						A704000027
A14	POWER SUPPLY ASSY						A704000034
A15	REPEATER WELL ASSY						A704000035
A16	EJECTOR DETAIL ASSY						A704000036

Table 7—2. 7040 Transmit Generator Assembly A2 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY B7040-00-020
PC ASSY 96836 XMITT QRSS PAGE 1 REV 03 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1-2	5600PF		2%	300V	ELMENCO	CM06FC562GO	335405620
C3-12	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C13	10UF		10%	10V	KEMET	T330A106K010AS	310001060
C14-15	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
CR1-2	DO35 4NS 10MA		SI	50UA	FAIRCHILD	IN4148	560041480
L1-2	56UH		5%		NYTRONICS	WEE-56	461000400
PC2	XMITT QRSS GENERATOR						970196836
Q1-2	TO-18 360MW TA NPN			15V	FAIRCHILD	2N2369A	550023691
Q3	TO-92 350MW TA NPN			25V	MOTOROLA	MPS6515	550065150
R3	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R4	26.7-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226791
R6	26.7-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226791
R7	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R10	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R11	26.7-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226791
R13	26.7-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226791
R14	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R15	100-	1/4W	10%		AB	TYPE CB	200101016
R16	2K	1/2	10%		HELIPOT	72XWR2K	232702027
R17-20	1.8K	1/4W	10%		AB	TYPE CB	200101826
R21	4870-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220248711
R22	3.3K	1/4W	10%		AB	TYPE CB	200103326
R23-24	750-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220275001
R25	3.3K	1/4W	10%		AB	TYPE CB	200103326
R26	4870-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220248711
R27-28	1.8K	1/4W	10%		AB	TYPE CB	200101826
T1	16DILP				ARTTED	AC8326	440200100
U1	14 DIP-P			LS	T.I.	SN74LS04N	510907404
U2	14 DIP-P			LS	T.I.	SN74LS00N	510907400
U3	14 DIP-P			LS	T.I.	SN74LS20N	510907420
U4	14 DIP-P			LS	T.I.	SN74LS164N	510974164
U5	14 DIP-P			LS	T.I.	SN74LS32N	510907432
U6	14 DIP-P			LS	T.I.	SN74LS74N	510907474
U7	14 DIP-P			LS	TI	SN74LS73N	510907473
U8	14 DIP-P			LS	T.I.	SN74LS164N	510974164
U9	14 DIP-P			LS	T.I.	SN74LS27N	510907427
U10	14 DIP-P			LS	T.I.	SN74LS21N	510907421
U11	14 DIP-P			LS	T.I.	SN74LS33N	510907433
U12	14 DIP-P			LS	T.I.	SN74LS164N	510974164
U13	14 DIP-P			LS	T.I.	SN74LS27N	510907427
U14	14 DIP-P			LS	T.I.	SN74LS86N	510907486
U15	14 DIP-P			LS	T.I.	SN74LS74N	510907474
U16	14 DIP-P			LS	T.I.	SN74LS21N	510907421

Table 7—3. 7040 QRSS Receiver Assembly A3 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY B7040-00-021
PC ASSY 96837 QRSS REC. PAGE 1 REV 00 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1-20	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
PC3	QRSS RECEIVER						970096837
U1-3	14 DIP-P				LS T.I.	SN74LS164N	510974164
U4	14 DIP-P				LS T.I.	SN74LS04N	510907404
U5	14 DIP-P				LS T.I.	SN74LS93N	510907493
U6-8	14 DIP-P				LS T.I.	SN74LS164N	510974164
U9	14 DIP-P				LS T.I.	SN74LS00N	510907400
U10	14 DIP-P				LS T.I.	SN74LS93N	510907493
U11	14 DIP-P				LS T.I.	SN74LS32N	510907432
U12-13	14 DIP-P				LS T.I.	SN74LS27N	510907427
U14	14 DIP-P				LS T.I.	SN74LS74N	510907474
U15	14 DIP-P				LS T.I.	SN74LS93N	510907493
U16	14 DIP-P				LS T.I.	SN74LS86N	510907486
U17	14 DIP-P				LS T.I.	SN74LS21N	510907421
U18	14 DIP-P				LS T.I.	SN74LS10N	510907410
U19	14 DIP-P				LS T.I.	SN74LS93N	510907493
U20	14 DIP-P				LS T.I.	SN74LS02N	510907402

Table 7—4. 7040 Interface Assembly A4 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY B7040-00-022
PC ASSY 96838 INTERFACE PAGE 1 REV 03 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1	10UF	B	10%	25V	SPRAGUE	196D106X9025KA1	310801061
C2	820 PF		5%	300V	ELMENCO	CM05-C821J0	335408210
C3	1 MF	A	20%	35V	SPRAGUE	196D105X0035HA1	310801050
C4	.1UF	A	20%	35V	SPRAGUE	196D104X0035HA1	310801040
C5	.01UF		1%	100V	FDYNE	PPA-11-.01-100-1	322401030
C6	1 MF	A	20%	35V	SPRAGUE	196D105X0035HA1	310801050
C9	22UF	B	10%	15V	SPRAGUE	196D226X9015KA1	310802263
C10-11	10UF	B	10%	25V	SPRAGUE	196D106X9025KA1	310801061
C12	22UF	B	10%	15V	SPRAGUE	196D226X9015KA1	310802263
C13-24	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
CR1-2	DO35 4NS 10MA SI 50UA				FAIRCHILD	IN4148	560041480
R1	1.8K	1/4W	10%		AB	TYPE CB	200101826
R2-4	4.7K	1/4W	10%		AB	TYPE CB	200104726
R5	1.8K	1/4W	10%		AB	TYPE CB	200101826
R6	1330-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220213311
R7	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R8	4.7K	1/4W	10%		AB	TYPE CB	200104726
R9	26.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226121
R10	4.7K	1/4W	10%		AB	TYPE CB	200104726
R11	4640-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220246411
R12	560-	1/4W	10%		AB	TYPE CB	200105616
R13	180-	1/4W	10%		AB	TYPE CB	200101816
R14	560-	1/4W	10%		AB	TYPE CB	200105616
R15	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R16	5.62K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220256211
R20-23	15K	1/4W	10%		AB	TYPE CB	200101536
SA2	SW,PEGRM,PCC,2 PCS,QSY5D				NO.ELECT	A0240089	640000801
SC	SW,PEGRM,PCC,2 PCS,QSY5D				NO.ELECT	A0240089	640000801
U1	14 DIP-P			LS	T.I.	SN74LS00N	510907400
U2	14 DIP-P			LS	T.I.	SN74LS05N	510907405
U3	14DIP-P			TTL	TI	SN7473N	510074730
U4	16-DIP-P			LS	T.I.	SN74LS157N	510974157
U5	14DIP-P			TTL	TI	SN7404N	510074040
U6	14 DIP				NAT.SEMI	LM339N	500000339
U7	14 DIP-P			LS	T.I.	SN74LS00N	510907400
U8	14 DIP-P			LS	T.I.	SN74LS10N	510907410
U9	14DIP-P			TTL	TI	SN7402N	510074020
U11-12	16DIP-P			DM3	FAIRCHILD	9602PC	510096025

Table 7—5. 7040 Clock Assembly A5 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY B7040-00-023
PC ASSY 56839 CLOCKS — PAGE 1 REV 04 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1	15UF		10%	10V	KEMET	T330A156K010AS	310001560
C2-4	100PF	CB N3300	10%	1KV	CENTRALAB	DD-101	330001010
C5-7	8-50PF			350V	ERIE	557-091E-8-50	340005000
C8-10	20PF		5%	100V	ELMENCO	CM04EA200JC	335402000
C11-13	47PF		5%	100V	ELMENCO	CM04-A470J0-	335404700
C14	10UF	B	10%	25V	SPRAGUE	196D106X9025KA1	310801061
C15	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C16	1500PF	DC Z5R	10%	1KV	CENTRALAB	DD-152	330001520
C17-25	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C26	20PF		5%	100V	ELMENCO	CM04EA200J0	335402000
C27	8-50PF			350V	ERIE	557-091E-8-50	340005000
C28	47PF		5%	100V	ELMENCO	CM04-A470J0-	335404700
C29	100PF	DB N3300	10%	1KV	CENTRALAB	DD-101	330001010
CRYSTAL	CRYSTAL INSULATOR						A704000119
L1	27UH		5%		NYTRONICS	WEE-27	461001300
Q1-8	TO-92 350MW TA NPN			40V	MOTOROLA	2N3903	550039030
Q4-6				** NO FIXFLE **			550003903
R1-3	470-	1/4W	10%		AB	TYPE CB	200104716
R4-6	2.2K	1/4W	10%		AB	TYPE CB	200102226
R7-9	4.7K	1/4W	10%		AB	TYPE CB	200104726
R10-12	56K	1/4W	10%		AB	TYPE CB	200105636
R19-21	1.8K	1/4W	10%		AB	TYPE CB	200101826
R22	82.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220282521
R23	11.3K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220211321
R24	56K	1/4W	10%		AB	TYPE CB	200105636
R25	2.2K	1/4W	10%		AB	TYPE CB	200102226
R26	4.7K	1/4W	10%		AB	TYPE CB	200104726
R27	470-	1/4W	10%		AB	TYPE CB	200104716
U1	14DIP-P			TTL	TI	SN7410N	510074100
U2	14DIP-P			S	T.I.	SN74S10	510807410
U3	14 DIP-P			LS	T.I.	SN74LS02N	510907402
U4	14 DIP-P			LS	T.I.	SN74LS00N	510907400
U5	FLIP-FLOP ADAP.BD.97058						A704000059
U6	14 DIP-P			LS	TI	SN74LS73N	510907473
U7	14 DIP-P			LS	T.I.	SN74LS04N	510907404
U8	16 DIP-P			LS	T.I.	SN74LS165N	510974165
U9	14 DIP-P			LS	TI	SN74LS73N	510907473
U10	8DIP-P			LM	SIGNETICS	NE 555V	510005550
Y1	CRYSTAL,6.176MHZ				VALPEY	6.176MHZ-VM6	919100005
Y2	CRYSTAL,9.48MHZ				VALPEY	9.48MHZ-VM6	919100006
Y3	CRYSTAL,12.608MHZ				VALPEY	12.608MHZ-VM6	919100007
Y4	CRYSTAL 6.178MHZ				VALPEY	6.178MHZ-V 6	919100015

Table 7—6. 7040 Flip Flop Adapter Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY B7040-00-059
FLIP-FLOP ADAP.BD.97058 PAGE 1 REV 01 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
J1	7 SIL				BERG	65500-107	654003429
J2	7 SIL				BERG	65500-107	654003429
U5	14 DIP-P			TTL	TI	SN74S113N	510074113

Table 7—7. 7040 T148 Generator Assembly A6 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY B7040-00-024
PC ASSY 56840 T148 GEN PAGE 1 REV 02 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1-17	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
PC6	T148 GENERATOR						970096840
R1-6	1.8K	1/4W	10%		AB	TYPE CB	200101826
U1	14 DIP-P			LS	T.I.	SN74LS02N	510907402
U2	14 DIP-P			LS	TI	SN74LS73N	510907473
U3	14 DIP-P			LS	T.I.	SN74LS74N	510907474
U4	14 DIP-P			LS	T.I.	SN74LS04N	510907404
U5	14 DIP-P			LS	T.I.	SN74LS164N	510974164
U6	14 DIP-P			LS	TI	SN74LS73N	510907473
U7	14 DIP-P			LS	T.I.	SN74LS74N	510907474
U8	16 DIP-P			LS	T.I.	SN74LS193N	510974193
U9	14 DIP-P			LS	T.I.	SN74LS27N	510907427
U10	T148 XMIT PROM						A704000046
U11	14 DIP-P			LS	T.I.	SN74LS10N	510907410
U12	14 DIP-P			LS	T.I.	SN74LS74N	510907474
U13	14 DIP-P			LS	T.I.	SN74LS00N	510907400
U14	14 DIP-P			LS	T.I.	SN74LS02N	510907402
U15	14 DIP-P			LS	T.I.	SN74LS00N	510907400
U16	14 DIP-P			LS	T.I.	SN74LS74N	510907474
U17	16 DIP-P			LS	T.I.	SN74LS161N	510974161
U18-19	14 DIP-P			LS	T.I.	SN74LS95N	510907495
XU10	16 DIP				BURNDY	DILB16P-108	820101100

Table 7—8. 7040 T148 Receiver Assembly A7 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY 87040-00-025
PC ASSY 96841 T148 REC — PAGE 1 REV 00 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1-14	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
PC-7	T148 RECEIVE						970096841
R1-8	1.8K	1/4W	10%		AB	TYPE CB	200101826
U1	14 DIP-P				LS T.I.	SN74LS04N	510907404
U2	14 DIP-P				LS T.I.	SN74LS10N	510907410
U3	16 DIP-P				LS T.I.	SN74LS174N	510974174
U4	T148 RECEIVE PROM						A704000047
U5	14 DIP-P				LS T.I.	SN74LS10N	510907410
U6	16 DIP-P				LS T.I.	SN74LS192N	510974192
U7	14 DIP-P				LS T.I.	SN74LS27N	510907427
U8	14 DIP-P				LS T.I.	SN74LS10N	510907410
U9	16 DIP-P				LS T.I.	SN74LS161N	510974161
U10	16-DIP-P				LS T.I.	SN74LS157N	510974157
U11	14 DIP-P				LS T.I.	SN74LS74N	510907474
U12	14 DIP-P				LS T.I.	SN74LS02N	510907402
U13	14 DIP-P				LS T.I.	SN74LS74N	510907474
U14	16 DIP-P				LS T.I.	SN74LS165N	510974165
XU4	16 DIP				BURNDY	DILB16P-108	820101100

Table 7—9. 7040 Digital Fault Locate Generator Assembly A8 Parts List.

N O R T H E A S T REPLACABLE PARTS LIST FOR ASSEMBLY B7040-00-026
E L E C T R O N I C S PC ASSY 96842 DIG FAULT PAGE 1 REV 03 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1-2	100PF		2%	500V	ARCO	CM04FD101G0	335401010
C3-10	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C11	8.2UF		10%	15V	KEMET	T330A825K015AS	310008250
C12	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C13	22UF		10%	6V	KEMET	T330A226K006AS	310002260
C14-17	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C18	1000PF		2%	100V	ELMENCO	CM06DA102G0	335401020
PC8	DIGITAL FAULT LOCATE						970196842
R1	7500-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220275011
R2	5.36K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220253611
R3	4.7K	1/4W	10%		AB	TYPE CB	200104726
R4-11	560-	1/4W	10%		AB	TYPE CB	200105616
R12	44.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220244221
R13	4.7K	1/4W	10%		AB	TYPE CB	200104726
R14	44.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220244221
R15-25	1.8K	1/4W	10%		AB	TYPE CB	200101826
R26	4.7K	1/4W	10%		AB	TYPE CB	200104726
R27	1.8K	1/4W	10%		AB	TYPE CB	200101826
R29	1.8K	1/4W	10%		AB	TYPE CB	200101826
R30-31	4.7K	1/4W	10%		AB	TYPE CB	200104726
R32	500K	1/2W	10%		HELIPOT	72XWR500K	232705044
U1	14 DIP-P			LS	T.I.	SN74LS00N	510907400
U2	16DIP-P			S	FAIRCHILD	96S02PC	510809602
U3	14 DIP-P			LS	T.I.	SN74LS74N	510907474
U4	14 DIP-P			LS	T.I.	SN74LS93N	510907493
U5	F.L. LOW-ORDER PROM						A704000049
U6	16DIP-P			LS	T.I.	SN74LS175N	510974175
U7	14 DIP-P			LS	T.I.	SN74LS00N	510907400
U8	14 DIP-P			LS	T.I.	SN74LS197N	510974197
U9	16DIP-P			TTL	TI	SN7445N	510074450
U10	F.L. HI-ORDER PROM						A704000048
U11	14 DIP-P			LS	T.I.	SN74LS93N	510907493
U12	14 DIP-P			LS	T.I.	SN74LS74N	510907474
U13	8DIP-P			LM	SIGNETICS	NE 555V	510005550
U14	14DIP-P			TTL	TI	SN7405N	510074050
U15	14DIP-P			TTL	TI	SN7410N	510074100
U16	14 DIP-P			LS	T.I.	SN74LS27N	510907427
U17	16 DIP-P			LS	T.I.	SN74LS76N	510907476
U18	14DIP-P			TTL	TI	SN7405N	510074050
U19-20	16 DIP-P			LS	T.I.	SN74LS163N	510974163
U21	14 DIP-P			LS	T.I.	SN74LS12N	510907412
U22	14 DIP-P			LS	T.I.	SN74LS10N	510907410
XU5	16 DIP				BURNDY	DILB16P-108	820101100
XU10	16 DIP				BURNDY	DILB16P-108	820101100

Table 7—10. 7040 Interconnection Assembly A9 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY B7040-00-028
PC ASSY 96843 INTERCONN. PAGE 1 REV 04 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
J2-8	TYPE 1F	22 DUAL MIL BLWS			AMPHENOL	225-22221-110	651701200
J11-12	10 DIL				BERG	65610-120	654003326
PC9	INTERCONNECTION BOARD						970396843
R1	180-	1/4W	10%		AB	TYPE CB	200101816
W1	FLAT CABLE RPTR TEST						A704000019
W2	FLAT CABLE ANALOG FAULT						A704000018

Table 7—11. 7040 Cable A9W1 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY B7040-00-019
FLAT CABLE RPTR TEST PAGE 1 REV 02 DATED 8/01/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
P1	34 PIN				3M	3402-0000T	654000101
P2	2 X 17				3M	3463-0001	654200034

Table 7—12. 7040 Cable A9W2 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY B7040-00-018
FLAT CABLE ANALOG FAULT PAGE 1 REV 01 DATED 8/01/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
P1	34 PIN				3M	3402-0000T	654000101
P2	2 X 17				3M	3463-0001	654200034

Table 7—13. 7040 Analog Fault Locate Assembly A10 Parts List.

N O R T H E A S T
E L E C T R O N I C S

REPLACABLE PARTS LIST FOR ASSEMBLY C7040-00-029
PC ASSY 96844 ANALOG PAGE 1 REV 09 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1-2	22UF	F	20%	35V	SPRAGUE	196D226X0035PE4	310802261
C3	22UF	B	10%	15V	SPRAGUE	196D226X9015KA1	310802263
C4-5	.01UF	00		50V	CENTRALAB	CK-103	330701030
C6	4.7UF	B	20%	35V	SPRAGUE	196D475X0035JA1	310804750
C7	1.0UF MD	Y5V	20%	50V	ERIE	8131-050-651-105M	330801050
C8-9	.01UF	00		50V	CENTRALAB	CK-103	330701030
C10	47 MF	G	20%	35V	SPRAGUE	196D476X0035TE4	310804760
C11-12	22UF	F	20%	35V	SPRAGUE	196D226X0035PE4	310802261
C13	47 MF	G	20%	35V	SPRAGUE	196D476X0035TE4	310804760
C14-21	.01UF	1%		100V	FDYNE	PPA-11-.01-100-1	322401030
C22-29	1.0UF MD	Y5V	20%	50V	ERIE	8131-050-651-105M	330801050
C30-31	22UF	B	10%	15V	SPRAGUE	196D226X9015KA1	310802263
C32	.01UF	00		50V	CENTRALAB	CK-103	330701030
C34-35	.01UF	00		50V	CENTRALAB	CK-103	330701030
C36	1.0UF MD	Y5V	20%	50V	ERIE	8131-050-651-105M	330801050
C37	.01UF	00		50V	CENTRALAB	CK-103	330701030
C38	.01UF	00		50V	CENTRALAB	CK-103	330701030
C39	22UF	F	20%	35V	SPRAGUE	196D226X0035PE4	310802261
C40	.01UF	00		50V	CENTRALAB	CK-103	330701030
C41	.56 UF	1%		200V	ELECTROCUBE	2308IC564F	322856420
C42	.30UF	1%		200V	ELECTROCUBE	2308IC304F	322830420
C44-45	.01UF	00		50V	CENTRALAB	CK-103	330701030
C47-48	.01UF	00		50V	CENTRALAB	CK-103	330701030
C49	1 MF	A	20%	35V	SPRAGUE	196D105X0035HA1	310801050
C50	510PF DB	Z5R	10%	1KV	CENTRALAB	DD-511	330005110
C51	.01UF	1%		100V	FDYNE	PPA-11-.01-100-1	322401030
C52	470PF	2%		500V	ELMENCO	CM05ED471G0	335404711
C53	.01UF	1%		100V	FDYNE	PPA-11-.01-100-1	322401030
C54	4700PF	2%		500V	ELMENCO	CM06ED472G0	335404720
C55	15PF DA	N330	10%	1KV	CENTRALAB	DD-150	330001500
CR1-7	DO35 4NS 10MA	SI	50UA		FAIRCHILD	IN4148	560041480
CR8-9	A140 1W	1%	7.5V		SCHAUER	SZ7.5	562000750
CR10-11	A1 300N 30P	SI	.1MA		TI	1N661	560006610
CR12-13	DO41 1A	SI	400V		EDAL	IN4004	560040040
CR16	DO35 4NS 10MA	SI	50UA		FAIRCHILD	IN4148	560041480
E1	PROTECTOR S/V GAS				SIEMENS	B1-C90/20	566009020
K1-2	RLY 1A 1B MUST CP4V				MICTEX	172100SB8	604103400
L1-2	100UH	5%			NYTRONICS	WEE-100	461000600
L3	150MH 22MA	2%			TRIAD	EA-150	460100200
Q1	TO-92 350MW TA	PNP		40V	MOTOROLA	MPS6518	550065180
Q2	TO-92 350MW TA	NPN		25V	MOTOROLA	MPS6515	550065150
Q3	TO92 350MW TC	PNP		50V	MOTOROLA	2N5087	552050870
Q4-6	TO-92 350MW TA	NPN		25V	MOTOROLA	2N5089	550050890
Q7	TO92 350MW TC	PNP		50V	MOTOROLA	2N5087	552050870
Q8	TO-92 350MW TA	NPN		25V	MOTOROLA	2N5089	550050890

Table 7—13. (Cont'd)

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY C7040-00-029
PC ASSY 56844 ANALOG — PAGE 2 REV 09 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
Q9-10	TO92	350MW TC PNP		50V	MOTOROLA	2N5087	552050870
R1	4990-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249911
R2	4120-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220241211
R3	6040-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220260411
R5	27K	1/4W	5%		A.B.	TYPE CB	200102735
R6	27K	1/4W	5%		A.B.	TYPE CB	200102735
R7	86.6K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220286621
R8	24.3K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220224321
R9	1540-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215411
R10	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R11	100K	1/2W	10%		BECKMAN	72XWR100K	232701043
R12	20K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220021
R13	1210-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220212111
R14	20K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220021
R15	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R16	4990-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249911
R17	9090-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220290911
R18	1000-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210011
R19	2K	1/2	10%		HELIPOT	72XWR2K	232702027
R20	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R21	1K	1/4W	10%		AB	TYPE CB	200101026
R22	56-	1/4W	10%		AB	TYPE CB	200105606
R23-24	1K	1/4W	10%		AB	TYPE CB	200101026
R25	56-	1/4W	10%		AB	TYPE CB	200105606
R26	1K	1/4W	10%		AB	TYPE CB	200101026
R27	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R28	8.87K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220288711
R29	1.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220214011
R30-32	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R33	19.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220219121
R34	100-	1/4W	10%		AB	TYPE CB	200101016
R35	8.87K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220288711
R36-37	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R38	23.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220223721
R39-40	100-	1/4W	10%		AB	TYPE CB	200101016
R41	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R42	200K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220031
R43	34K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234021
R44	4220-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220242211
R45	100-	1/4W	10%		AB	TYPE CB	200101016
R46	13.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220213721
R47	14.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220214721
R48	15K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215021
R49	2K	1/2	10%		HELIPOT	72XWR2K	232702027
R50	316K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220231631
R51	100K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210031
R52	30.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220230921
R53	9090-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220290911
R54	2210-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220222111
R55	12.1-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220212191
R56	750-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220275001
R57	500-	1/2	10%		HELIPOT	72XWR500	232705017

Table 7—13. (Cont'd)

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY C7040-00-029
PC ASSY 96844 ANALOG — PAGE 3 REV 09 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
R58	90.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220290921
R59-62	2.2K	1/4W	10%		AB	TYPE CB	200102226
R63-74	1.8K	1/4W	10%		AB	TYPE CB	200101826
R75-76	560-	1/4W	10%		AB	TYPE CB	200105616
R77	35.2K	1/8W	.5%		ELECTRA	RN55 SIZE 50 PPM	222435227
R78	56.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220256221
R79-81	2.2K	1/4W	10%		AB	TYPE CB	200102226
R82	1M	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210041
R83	29.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220229421
R84	43.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220243221
R85	18.2K	1/8W	.5%		ELECTRA	RN55 SIZE 50 PPM	222418227
R86	25.2K	1/8W	.5%		ELECTRA	RN55 SIZE 50 PPM	222425227
R87	20.0K	1/8W	.5%		ELECTRA	RN55 SIZE 50 PPM	222420027
R88	22.3K	1/8W	.5%		ELECTRA	RN55 SIZE 50 PPM	222422327
R89	49.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249921
R90	100K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210031
R91	1000-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210011
R92	51.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220251121
R93	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R94	51.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220251121
R95	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R96	787-	108W	1%		ELECTRA	RN55 SIZE 100 PPM	220278701
R98	900-	3W	1%		TEL LAB	EL2B	210390001
R99	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R100	21.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220221521
R101	45.3K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220245321
R102	4990-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249911
R103	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R104	49.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249921
R105	PC BD MTG W/POT 10K				OAK	5-18741-767	625000408
R106	47.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220247521
R107	42.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220242221
R108	37.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220237421
R109	32.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220232421
R110	29.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220229421
R111	26.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226121
R112	22.6K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220222621
R113	19.6K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220219621
R114	17.8K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220217821
R115	16.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220216221
R116	14.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220214721
R117	13K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220213021
R118	93.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220293121
R119	82.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220282521
R120	73.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220273221
R121	63.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220263421
R122	57.6K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220257621
R123	51.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220251121
R124	44.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220244221
R125	38.3K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220238321

Table 7—13. (Cont'd)

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY C7040-00-029
PC ASSY 56844 ANALOG — PAGE 4 REV 09 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
R126	34.8K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234821
R127	32.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220232421
R128	28.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220228721
R129	25.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220225521
R130	16.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220216921
R131	15K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215021
R132	13.3K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220213321
R133	11.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220211521
R134	10.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210521
R135	9.31K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220293111
R136	8.06K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220280611
R137	6980-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220269811
R138	6340-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220263411
R139	5.76K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220257611
R140	5230-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220252311
R141	4640-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220246411
R142	56.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220256221
R143	49.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249921
R144	44.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220244221
R145	38.3K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220238321
R146	34.8K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234821
R147	30.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220230921
R148	27.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220227421
R149	23.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220223221
R150	21K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220221021
R151	19.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220219121
R152	17.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220217421
R153	15.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215421
S1	PC BD MTG W/POT 10K				OAK	5-18741-767	625000408
S2	PC BD MTG 5D-1CKT-12POS				OAK	625000412	625000412
S3	DPDT	5A		28V	C+K COMP	7201P3YZB	620400600
T1	TRANSFORMER,INPUT				MIDCOM	671-0215	400100002
T2	TRANSFORMER,INPUT				ADC	BUG-4-0020	400100001
U1-3	8PDIL				NAT. SEMI	LM741CN	500007412
U4	8PDIL	80MW		180V	NAT.SEMI	LM1458N	500001458
U5-6	16 DIP-P	8		CMOS	RCA	CD4051BE	510004051
U7-8	8PDIL	80MW		180V	NAT.SEMI	LM1458N	500001458
U9	10P TO-5				RCA	CA3019T	500030190
U10	14 DIP				RAYTHEON	RC4136DB	500004136

Table 7—14. 7040 Artline Assembly All Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY C7040-00-030
PC ASSY 96845 ART.LINE — PAGE 1 REV 06 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1-3	22UF	F	20%	35V	SPRAGUE	196D226X0035PE4	310802261
C4	39 PF		2%	500V	ELMENCO	CM04ED390G03	335403901
C5	270PF		2%	300V	ELMENCO	CM04EC271G0	335402711
C6	47PF		2%	500V	ELMENCO	CM04ED470G0	335404701
C7-9	.1UF	MD W5R	10%	50V	USCC	CW30C104K	330801041
C10	39 PF		2%	500V	ELMENCO	CM04ED390G03	335403901
C11	270PF		2%	300V	ELMENCO	CM04EC271G0	335402711
C12	47PF		2%	500V	ELMENCO	CM04ED470G0	335404701
C13-15	.1UF	MD W5R	10%	50V	USCC	CW30C104K	330801041
C16	39 PF		2%	500V	ELMENCO	CM04ED390G03	335403901
C17	270PF		2%	300V	ELMENCO	CM04EC271G0	335402711
C18	47PF		2%	500V	ELMENCO	CM04ED470G0	335404701
C19-21	.1UF	MD W5R	10%	50V	USCC	CW30C104K	330801041
C22	39 PF		2%	500V	ELMENCO	CM04ED390G03	335403901
C23	270PF		2%	300V	ELMENCO	CM04EC271G0	335402711
C24	47PF		2%	500V	ELMENCO	CM04ED470G0	335404701
C25	.1UF	MD W5R	10%	50V	USCC	CW30C104K	330801041
C26-27	.1UF	MD W5R	10%	50V	USCC	CW30C104K	330801041
C28	12PF		5%	500V	ELMENCO	CM04ED120J0	335401200
C29-30	30PF		2%	500V	ELMENCO	CM04ED300G0-	335403000
C31	36PF		2%	500V	ELMENCO	CM04ED360G0	335403600
C32	100PF		2%	500V	ARCO	CM04FD101G0	335401010
C33	43PF		2%	500V	ELMENCO	CM04ED430G0	335404300
C34	47PF		2%	500V	ELMENCO	CM04ED470G0	335404701
C35	130 PF		2%	500V	ELMENCO	CM04ED131G03	335401211
C36	68PF		2%	100V	ELMENCO	CM04DA680G0	335406800
C37	56PF		2%	500V	ELMENCO	CM04ED560G03	335405600
C38	200 PF		2%	500V	ELMENCO	CM04ED201G03	335402011
C39	91 PF		2%	500V	ELMENCO	CM04ED910G03	335409100
C40	62PF		2%	500V	ELMENCO	CM04ED620G03	335406201
C41	240PF		2%	500V	ELMENCO	CM04ED241G03	335402410
C42-48	.1UF	MD W5R	10%	50V	USCC	CW30C104K	330801041
C49	2.2UF	ME Y5V	20%	50V	ERIE	8141-050-651-225M	330802250
C50	75 PF		5%	100V	ELMENCO	CM05CA750J	335407500
C51	68PF		2%	100V	ELMENCO	CM04DA680G0	335406800
C52-55	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C56	39 PF		2%	500V	ELMENCO	CM04ED390G03	335403901
C57	200 PF		2%	500V	ELMENCO	CM04ED201G03	335402011
C58	75 PF		5%	100V	ELMENCO	CM05CA750J	335407500
C59	430 PF		5%	100V	ELMENCO	CM05CA431J	335404310
C60	50PF		2%	500V	ELMENCO	CM04ED500G0	335405000
C61	270PF		2%	300V	ELMENCO	CM04EC271G0	335402711
C62-63	.1UF		10%	35V	KEMET	T330A104K035AS	310001041
C64	100PF		2%	500V	ARCO	CM04FD101G0	335401010
C68-71	30PF		2%	500V	ELMENCO	CM04ED300G0-	335403000
C72-73	1UF		10%	35V	KEMET	T330A105K035AS	310001051
C74	.01UF		00	50V	CENTRALAB	CK-103	330701030
C75	.1UF	MD W5R	10%	50V	USCC	CW30C104K	330801041
CR1-2	A1AY	1W	10%	5.1V	MOTOROLA	1N4733	562047330
J1	10 SIL				BERG	65500-110	654003426
J2	2 SIL				BERG	65500-102	654003434

Table 7—14. (Cont'd)

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY C7040-00-030
PC ASSY 96845 ART.LINE — PAGE 2 REV 06 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
L1	100UH		5%		NYTRONICS	WEE-100	461000600
L2	270UH		5%		NYTRONICS	WEE-270	461000900
L3	56UH		5%		NYTRONICS	WEE-56	461000400
L5	560 UH		5%		NYTRONICS	WEE 560	461000001
L6	100UH		5%		NYTRONICS	WEE-100	461000600
L7	390UH		5%		NYTRONICS	WEE-390	461001100
L8	68 UH		5%		NYTRONICS	WEE-68	461000004
L9-10	100UH		5%		NYTRONICS	WEE-100	461000600
Q1-2	TO-92	350MW	TA NPN	25V	MOTOROLA	MPS6515	550065150
Q3-4	TO92	350MW	TC PNP	25V	MOTOROLA	MPS6519	552065190
Q5	TO-92	350MW	TA NPN	40V	MOTOROLA	2N3903	550039030
Q6	TO-92	350MW	TA NPN	25V	MOTOROLA	MPS6515	550065150
Q7	TO-92	350MW	TA NPN	40V	MOTOROLA	2N3903	550039030
R2-3	5110-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220251111
R4	27.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220227421
R5	5110-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220251111
R6	3010-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220230111
R7-8	20K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220021
R9	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R10	5110-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220251111
R11	27.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220227421
R12	10.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210721
R13	28.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220228721
R14	5110-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220251111
R15	3010-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220230111
R16-17	20K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220021
R18	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R19	5110-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220251111
R20	27.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220227421
R21	10.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210721
R22	28.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220228721
R23	5110-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220251111
R24	3010-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220230111
R25-26	20K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220021
R27	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R28	5110-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220251111
R29	27.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220227421
R30	10.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210721
R31	28.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220228721
R32	5110-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220251111
R33	3010-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220230111
R34-35	20K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220021
R36	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R37	1.24K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220212411
R38	2550-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220225511
R39	2430-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220224311
R40	12.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220212121
R41	2320-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220223211

Table 7—14. (Cont'd)

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY C7040-00-030
PC ASSY 96845 ART.LINE — PAGE 3 REV 06 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
R42	6650-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220266511
R43	27.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220227421
R44	2.26K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220222611
R45	5900-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220259011
R46	23.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220223721
R47	2210-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220222111
R48	5.62K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220256211
R49	22.6K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220222621
R50	2210-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220222111
R51	5490-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220254911
R52	20K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220021
R53	5110-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220251111
R56	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R57-58	10.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210721
R59	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R60	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R61-62	10-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210051
R63	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R64	10.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210721
R65	28.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220228721
R66	20.5-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220551
R67	18.2-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220218251
R68	16.5-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220216551
R69	14.7-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220214751
R70	118-	1/8W	1%		VARIOUS	RN55 SIZE 100PPM	220211801
R71	56.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220256221
R72	2210-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220222111
R73	4.7K	1/4W	10%		AB	TYPE CB	200104726
R74	470-	1/4W	10%		AB	TYPE CB	200104716
R75-77	1K	1/4W	10%		AB	TYPE CB	200101026
R78-80	5K	.75W	10		HELIPOT	89PR5K	232505020
R81	6.8K	1/4W	5%		AB	TYPE CB	200106825
R82	12K	1/4W	5%		AB	TYPE CB	200101235
R83	38.3-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220238351
R84	34.8-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234851
R85	31.6-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220231651
R86	28.7-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220228751
R87	25.5-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220225551
R88	23.2-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220223251
S1	PC BD MTG 1D-3CKT-3POS				OAK	625000410	625000410
S2	PC BD MTG 2D-1CKT-12PCS				OAK	625000409	625000409
S3	SWITCH,ROTARY				OAK	625000413	625000413
T1-2	16DILP				ARTTED	AC8326	440200100
U1-U5	OP.AMP	7295705CM8			NATIONAL	LM318N	500000318
U6	14 DIP-P			LS	T.I.	SN74LS93N	510907493
U7	14 DIP-P			LS	T.I.	SN74LS92N	510907492
U8	14 DIP-P			LS	T.I.	SN74LS93N	510907493
U9	14 DIP-P			LS	T.I.	SN74LS33N	510907433
Y1	CRYSTAL,9.24MHZ				VALPEY	9.238MHZ-VM6	915100008

Table 7—15. 7040 Front Panel Assembly A12 Parts List.

N O R T H E A S T REPLACABLE PARTS LIST FOR ASSEMBLY D7040-00-033
E L E C T R O N I C S FRONT PANEL ASSY PAGE 1 REV 04 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1	.1UF CO	Z5U	20%	500V	SPRAGUE	56A-P10	330401040
DS1-8		10 MA			H.PACKARD	5082-4658	564500801
DS9	LED,HI EFF.GREEN				H.P.	5082-4958	564500807
DS10-11		10 MA			H.PACKARD	5082-4658	564500801
DS12	LED,HI EFF.YELLOW				H.P.	5082-4558	564500806
F1		1A		250V	BUSSMAN	MDL	863101400
J1	CONN, 1-PIN FEM.PANEL MT				AMPHENOL	UG-625/U	653400400
J2	N/P				SWCRFT	5J-1594	650403200
J3	CKT 38				TEC.COMP		650400005
J4	N/P				SWCRFT	5J-1594	650403200
J5	MT3328				SWCRFT	5J-1583	650403100
J6	N/P				SWCRFT	5J-1594	650403200
J7-9	JACK,BANTAM				ADC	PJ839TS	650000001
M1	500 VA				JEWELL	73T/SPECIAL/	900000003
P4	6 COND				AMP	1-480270-0	650800200
R1	10K				AB	MA2G040S103UA	232001032
R2	510K	1/4W	10%		AB	TYPE CB	200105146
R3-4	430-	1/2W	5%		AB	TYPE EB	200204315
R5	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
S1	SELECTOR SWITCH ASSY						A704000044
S2	NEON			110V	DIALCO	913-1433-1631-525	630701200
S3	SPDT	5A		28V	C+K COMP	7101P3YZB	620400100
S4	4PDT	5A			C&K	7405P3DZB	620401701
S5	DPDT	5A		28V	C+K COMP	7213P3YZB	620401100
S6	SPDT	5A		28V	C+K COMP	7103P3DZB	620400300
W1	HARNESS LAYOUT FRT PNL 1						A704000012
W2	HARNESS LAYOUT JACK						A704000015
W3		6 A		250V	J.PHILIPS	13E89	932000802
XDS1-8	LED MTG. CLIP FOR T1 3/4				VISUAL COM	CLF-280-RTP	850501101
XDS9	LED MTG. CLIP FOR T1 3/4				VISUAL COM	CLF-280-GTP	850501102
XDS10-11	LED MTG. CLIP FOR T1 3/4				VISUAL COM	CLF-280-RTP	850501101
XDS12	LED MTG. CLIP FOR T1 3/4				VISUAL COM	CLF-280-YTP	850501103
XF1	FUSEHOLDER,3AG PANEL				BUSSMAN	HKF	863000100

Table 7—16. 7040 Cable A12W1 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY C7040-00-012
HARNESS LAYOUT FRT PNL 1 PAGE 1 REV 01 DATED 8/01/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
P1	20DILP				BERG	65043027	652001100
P2	6 COND				AMP	1-480270-0	650800200
P3	20DILP				BERG	65043027	652001100

Table 7—17. 7040 Cable A12W2 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY C7040-00-015
HARNESS LAYOUT JACK PAGE 1 REV 02 DATED 8/01/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
P1	10 SIL				BERG	65039-027	652002025

Table 7—18. 7040 Repeater Test Assembly A13 (C7040-00-027) Parts List.

N O R T H E A S T E L E C T R O N I C S — REPLACABLE PARTS LIST FOR ASSEMBLY C7040-00-027
PC ASSY 56997 RPTR TEST — PAGE 1 REV 08 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1	10UF		10%	10V	KEMET	T330A106K010AS	310001060
C2	.1UF	MC Y5V	20%	50V	ERIE	8121-050-651-104M	330801040
C3	.1UF	DO Z5U	20%	500V	SPRAGUE	5GA-P10	330401040
C4	22UF	F	20%	35V	SPRAGUE	196D226X0035PE4	310802261
C5	1UF		10%	35V	KEMET	T330A105K035AS	310001051
C6	1UF		10%	35V	KEMET	T330A105K035AS	310001051
C7	1UF		10%	35V	KEMET	T330A105K035AS	310001051
C8	22UF	F	20%	35V	SPRAGUE	196D226X0035PE4	310802261
C9	.1UF		10%	35V	KEMET	T330A104K035AS	310001041
C10-13	1UF		10%	35V	KEMET	T330A105K035AS	310001051
C14	30 PF	CA N330	10%	1KV	CRL	DD-300	330003000
C17-22	.1UF	MC Y5V	20%	50V	ERIE	8121-050-651-104M	330801040
C23	1UF		10%	35V	KEMET	T330A105K035AS	310001051
CR1	D041	1A	SI	200V	EDAL	1N4003	560040030
CR2	D041	1A	SI	200V	EDAL	1N4003	560040030
CR3	A1AY	1W	5%	15V	MOTOROLA	1N4744A	562047440
CR4	A1AY	1W	10%	5.1V	MOTOROLA	1N4733	562047330
CR5-8	D041	1A	SI	800V	EDAL	1N4006	560040060
CR9	A1EE	5W	5%	7.5V	MOTOROLA	1N5343B	562053432
CR10	D041	1A	SI	200V	EDAL	1N4003	560040030
CR11	D041	1A	SI	200V	EDAL	1N4003	560040030
CR16	A1EE	5W	5%	7.5V	MOTOROLA	1N5343B	562053432
CR17	A1AY	1W	10%	5.1V	MOTOROLA	1N4733	562047330
CR18	A1AY	1W	10%	5.1V	MOTOROLA	1N4733	562047330
CR19	D035 4NS	10MA	SI	50UA	FAIRCHILD	IN4148	560041480
CR20	D035 4NS	10MA	SI	50UA	FAIRCHILD	IN4148	560041480
J2	13 DIL				BERG	65610-126	654003323
J3-4	10 SIL				BERG	65500-110	654003426
K1	RELAY,REED,LO-CROSS TALK				MICTEX	172-200SD6	604100501
K2	RELAY,REED,LO-CROSS TALK				MICTEX	172-200SD6	604100501
K3	RLY 1A 1B MUST OP4V				MICTEX	172100SB8	604103400
K4	RELAY,REED,LO-CROSS TALK				MICTEX	172-200SD6	604100501
K5	RELAY,REED,LO-CROSS TALK				MICTEX	172-200SD6	604100501
L1	100UH		5%		NYTRONICS	WEE-100	461000600
L2	150UH		5%		NYTRONICS	WEE-150	461000700
L3	100UH		5%		NYTRONICS	WEE-100	461000600
Q1	TO-92 350MW TA	NPN		25V	MOTOROLA	MPS6515	550065150
Q2	TO-92 350MW TA	NPN		40V	MOTOROLA	2N3903	550039030
Q3	TO-92 350MW TA	NPN		40V	MOTOROLA	2N3903	550039030
Q4	TO-106 250MW TA	PNP		12V	NATIONAL	2N4258A	552042581
Q5	TO-106 250MW TA	NPN		12V	NATIONAL	2N4274	550042740
Q6	TO-106 250MW TA	PNP		12V	NATIONAL	2N4258A	552042581
Q7	TO-106 250MW TA	NPN		12V	NATIONAL	2N4274	550042740
R1	430-	1/4W	5%		AB	TYPE CB	200104315
R2	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001

Table 7—18. (Cont'd)

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY C7040-00-027
PC ASSY 56997 R&TR TEST PAGE 2 REV 08 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
R3	22.6K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220222621
R4	750-	1/4W	5%		AB	TYPE CB	200107515
R5	1K	1/2	10%		HELIPOT	72XWR1K	232701028
R6	300-	3W	10%		IRC	PW3	210303016
R7	2.2K	1/4W	10%		AB	TYPE CB	200102226
R8	10-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210051
R9	267-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226701
R10	316-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220231601
R11	267-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226701
R12	267-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226701
R13	316-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220231601
R14	267-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226701
R15	422-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220242201
R16	36.5-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220236551
R17	36.5-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220236551
R18	10-	3W	5%		W LEONARD	TYPE 3X	210301005
R19	10-	3W	5%		W LEONARD	TYPE 3X	210301005
R20	10-	3W	5%		W LEONARD	TYPE 3X	210301005
R21	10-	3W	5%		W LEONARD	TYPE 3X	210301005
R22	49.9-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249951
R23	49.9-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249951
R24	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R25	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R26	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R27	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R28	430-	1/4W	5%		AB	TYPE CB	200104315
R29	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R30	3400-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234011
R31	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R32	10-	2W	1%		TEL LAB	EL-2H	210210051
R33	20.5K	1/4W	1%		ELECTRA	RN60 SIZE 100 PPM	220520521
R34	102-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210201
R35	750-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220275001
R36	220-	1/4W	10%		AB	TYPE CB	200102216
R39	68K	1/4W	10%		AB	TYPE CB	200106836
R40	330-	1/4W	10%		AB	TYPE CB	200103316
R41	37.4-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220237451
R42	47K	1/4W	10%		AB	TYPE CB	200104736
R43	40.2-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220240251
S4	PC BD MTG 6D-12CKT-4PCS				OAK	625000411	625000411
T1	16DILP				ARTTED	AC8326	440200100
T2	LOC2MH				PRCFILE	4401-01-2818	440100100
T3	16DILP				ARTTED	AC8326	440200100
T4	16DILP				ARTTED	AC8326	440200100
T5	16DILP				ARTTED	AC8326	440200100
T6	16DILP				ARTTED	AC8326	440200100
U1	14DIP-P			TTL	TI	SN7402N	510074020
U2	14DIP-P			TTL	TI	SN7402N	510074020
U3-5	14 DIP-P				NATIONAL	LM361N	500003610
U6	8 DIP-P				NATIONAL	LM358N	500000358

Table 7—19. 7040 Repeater Test Assembly A13 (C7040-00-031) Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY 7040-00-031 CRYSTAL,9.24MHZ — PAGE REV 00 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C2	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C3	.1UF CO	Z5U	20%	500V	SPRAGUE	5GA-P10	330401040
C4	22UF	F	20%	35V	SPRAGUE	196D226X0035PE4	310802261
C5	10UF		10%	10V	KEMET	T330A106K010AS	310001060
C6	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C7	1UF		10%	35V	KEMET	T330A105K035AS	310001051
C8	22UF	F	20%	35V	SPRAGUE	196D226X0035PE4	310802261
C9	.1UF		10%	35V	KEMET	T330A104K035AS	310001041
C10-13	1UF		10%	35V	KEMET	T330A105K035AS	310001051
C14	30 PF CA	N330	10%	1KV	CRL	DD-300	330003000
CR1-2	D041	1A SI		200V	EDAL	1N4003	560040030
CR3	A1AY	1W	5%	15V	MOTOROLA	1N4744A	562047440
CR4	A1AY	1W	10%	5.1V	MOTOROLA	1N4733	562047330
CR5-8	BV 7.35V		5%		GEN SEMI	GZ60309A	565500003
CR9	OUTL.15	250MW		100P	H PACKARD	5082-2800	561550820
CR10-11	D041	1A SI		200V	EDAL	1N4003	560040030
J2	13 DIL				BERG	65610-126	654003323
J3-4	10 SIL				BERG	65500-110	654003426
K1-2	RELAY,REED,LO-CROSS TALK				MICTEX	172-200SD6	604100501
K3	RLY 1A 1B MUST OP4V				MICTEX	172100SB8	604103400
K4-5	RELAY,REED,LO-CROSS TALK				MICTEX	172-200SD6	604100501
L1	100UH		5%		NYTRONICS	WEE-100	461000600
L2	150UH		5%		NYTRONICS	WEE-150	461000700
L3	100UH		5%		NYTRONICS	WEE-100	461000600
PC12	REPEATER TEST BD						970296846
Q1	TO-92 350MW TA NPN			25V	MOTOROLA	MPS6515	550065150
Q2-3	TO-92 350MW TA NPN			40V	MOTOROLA	2N3903	550039030
Q4	TO-106 250MW TA PNP			12V	NATIONAL	2N4258A	552042581
Q5	TO-106 250MW TA NPN			12V	NATIONAL	2N4274	550042740
Q6	TO-106 250MW TA PNP			12V	NATIONAL	2N4258A	552042581
Q7	TO-106 250MW TA NPN			12V	NATIONAL	2N4274	550042740
Q8-9	TO-18 360MW TA NPN			15V	FAIRCHILD	2N2369A	550023691
R1	430-	1/4W	5%		AB	TYPE CB	200104315
R2	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R3	22.6K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220222621
R4	750-	1/4W	5%		AB	TYPE CB	200107515
R5	1K	1/2	10%		HELIPOT	72XWR1K	232701028
R6	300-	3W	10%		IRC	PW3	210303016
R7	2.2K	1/4W	10%		AB	TYPE CB	200102226
R8	10-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210091
R9	267-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226701
R10	316-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220231601
R11-12	267-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226701
R13	316-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220231601

Table 7—19. (Cont'd)

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY 7040-00-031
CRYSTAL,5.24MHZ — PAGE 5 REV 00 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
R14	267-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226701
R15	422-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220242201
R16-17	36.5-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220236591
R18-21	10-	3W	5%		W LEONARD	TYPE 3X	210301005
R22-23	307-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220230701
R24	5110-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220251111
R25	1470-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220214711
R26-27	2.2K	1/4W	10%		AB	TYPE CB	200102226
R28	430-	1/4W	5%		AB	TYPE CB	200104315
R29	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R30	3400-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234011
R31	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R32	10-	2W	1%		TEL LAB	EL-2H	210210091
R33	20.5K	1/4W	1%		ELECTRA	RN60 SIZE 100 PPM	220520521
R34	102-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210201
R35	750-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220275001
R36	220-	1/4W	10%		AB	TYPE CB	200102216
S1	PC BD MTG 6D-12CKT-4PCS				OAK	625000411	625000411
T1	16DILP				ARTTED	AC8326	440200100
T2	LOC2MH				PROFILE	4401-01-2818	440100100
T3-6	16DILP				ARTTED	AC8326	440200100
U1-2	14DIP-P				TTL TI	SN7402N	510074020

Table 7—20. 7040 Overall Power Supply Assembly A14 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY D7040-00-034
POWER SUPPLY ASSY — PAGE 1 REV 03 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
A1	PC ASSY 96847 PWR SUPPLY						A704000032
J1	6 COND				AMP	1-480271-0	650800100
Q1	MODT0220	65W	TC PAP	80V	T.I.	TIP42B	552000422
T1	XFMR,PWR,7040				NESHAMINY	PH-870-40	420500002
U1		3A		5V	NATIONAL	LM323K	500000323
U2	TO-220			+15V	FAIRCHILD	UA7815UC	500078150
U3	TO-220			-15V	FAIRCHILD	UA7915UC	500078151

Table 7—21. 7040 Power Supply Regulator Assembly A14A1 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY C7040-00-032
PC ASSY 96847 PWR SUPPLY PAGE 1 REV 04 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1	4000UF			15V	SPRAGUE	39D408G015JL4	300004081
C2	1UF		10%	35V	KEMET	T330A105K035AS	310001051
C3	10UF		10%	25V	KEMET	T330C106K025A	310001061
C4-5	500UF			50V	SPRAGUE	39D507G050GL4	300005071
C6-7	1UF		10%	35V	KEMET	T330A105K035AS	310001051
C8-9	10UF		10%	25V	KEMET	T330C106K025A	310001061
C10	1000UF			75V	SPRAGUE	39D108G075JP4	300001081
C11	500UF			50V	SPRAGUE	39D507G050GL4	300005071
C12	2.2UF		10%	35V	KEMET	T330A225K035AS	310002250
C13	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C14	4UF			350V	SPRAGUE	39D405F350EE4	300004050
C16	4000UF			15V	SPRAGUE	39D408G015JL4	300004081
C17	500PF DB	Z5F	10%	1KV	CRL	DD-501	330005010
C18	.47UF		10%	50V	KEMET	T330A474K050AS	310004741
CR1-4	A3Q	3A SI		100V	WSTNGHOUSE	1N5401	560054010
CR5-18	D041	1A SI		200V	EDAL	1N4003	560040030
CR20	D041	1A SI		400V	EDAL	IN4004	560040040
J1	16 COND				AMP	350214-1	650900900
J2-3	6PIN				AMP	1-380999-0	654002700
PC13	POWER SUPPLY BD						970296847
Q1	TO-5	1W TA NPN		65V	RCA	2N2102	550021020
R1-2	1.5K	3W	5%		W LEONARD	TYPE 3X	210301525
R3	50K	1/2W	10%		BECKMAN	72XWR50K	232705033
R4	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R5	3.9K	1/4W	10%		AB	TYPE CB	200103926
R6	1K	1/2W	10%		AB	TYPE EB	200201026
R7	120K	1W	5%		OHMITE	LITTLE DEVIL	200701245
R8	6.8K	1/4W	10%		AB	TYPE CB	200106826
R9	3-	3W	5%		W LEONARD	TYPE 3X	210303095
R10	47K	1/4W	10%		AB	TYPE CB	200104736
R11	22K	1/2W	10%		AB	TYPE EB	200202236
U1	TO-92	100 MA	5%	+5V	NATIONAL	LM78L05ACZ	500078053
U2	8 DIP-P				NATIONAL	LM358N	500000358

Table 7—22. 7040 Repeater Well Assembly A15 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY C7040-00-035
REPEATER WELL ASSY PAGE 1 REV 03 DATED 7/16/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
J1	TYPE 4G	10 SNGL MIL		TUFR	METHODE	91-6010-1100	651702002
J2	TYPE 1A	12 DUAL MIL		BLWS	AMPHENOL	225-21221-101	651700001
W1	HARNESS LAYOUT RPTR TEST						A704000017

Table 7—23. 7040 Cable A15W1 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY C7040-00-017
HARNESS LAYOUT RPTR TEST PAGE 1 REV 03 DATED 8/01/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
P1	26DILP				BERG	65043-024	652001500
P2	6 COND				AMP	1-480270-0	650800200

Table 7—24. 7040 Repeater Insert 7040-50 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY C7040-50-001
O/A ASSY RPTR INSERT PAGE 1 REV 01 DATED 8/01/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
P1	10PIN PANEL PLUG				AMPHENOL	133-010-21-101	651702101
P2	11-PIN MALE				GTELENKURT	041-48973-02	653500100

Table 7—25. 7040 Repeater Insert 7040-51 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY C7040-51-001
O/A ASSY RPTR INSERT PAGE 1 REV 00 DATED 8/01/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
J2	12 POS 150 CTRS				DYNATECH	46017-01-12-31	653500300
P1	10PIN PANEL PLUG				AMPHENOL	133-010-21-101	651702101

Table 7—26. 7040 Repeater Insert 7040-52 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY C7040-52-001
O/A ASSY RPTR. INDEP. PAGE 1 REV 02 DATED 8/01/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
J2	TYPE 4G 12 SNGL MIL TUFR				AMPHENOL	143-012-01	651702000
P1	10PIN PANEL PLUG				AMPHENOL	133-010-21-101	651702101

Table 7—27. 7040 Repeater Insert 7040-53 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY C7040-53-001
O/A ASSY RPTR 218/219 PAGE 1 REV 02 DATED 8/01/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
J2	CONN,PC EDGE 12POS DUAL				MICROTRON.	SQ-150-24-TS	651800009
P1	10PIN PANEL PLUG				AMPHENOL	133-010-21-101	651702101

Table 7—28. 7040 Repeater Insert 7040-54 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY D7040-54-001
O/A ASSY 206 RPTR INSERT PAGE 1 REV 07 DATED 8/01/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
F1		.3A		250V	LITTELFUSE	3AG	863100200
R1	150-	50W	1%		RCL	AL50-150	210601510
S1	3PDT				C&K	7301P3Y1ZB	620401201
XF1	FUSEHOLDER 3AG CHASSIS				LITTELFUSE	357001	863000200

Table 7—29. 7040 Repeater Insert 7040-55 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY D7040-55-001
O/A ASSY WECO 220 ADAPTOR PAGE 1 REV 02 DATED 8/01/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
F1		.3A		250V	LITTELFUSE	3AG	863100200
J1	CARD EDGE CONNECTOR				CONTRL DAT	VPB01D28A001	651800006
P1	10PIN PANEL PLUG				AMPHENOL	133-010-21-101	651702101
R1	210-	25W	1%		RCL	AL25-210	210602110
S1	4PDT				C&K	7401P3Y1ZB	620401601
XF1	FUSEHOLDER 3AG CHASSIS				LITTELFUSE	357001	863000200

Table 7—30. 7040 Repeater Insert 7040-57 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY C7040-57-001
O/A ASSY RPTR INSERT PAGE 1 REV 01 DATED 8/01/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
P1	10PIN PANEL PLUG				AMPHENOL	133-010-21-101	651702101
P2	11-PIN MALE				GTELENKURT	041-48973-02	653500100

Table 7—31. 7040 Repeater Insert 7040-58 Parts List.

NORTHEAST ELECTRONICS — REPLACABLE PARTS LIST FOR ASSEMBLY D7040-58-001
O/A ASSY RPTR INSERT PAGE 1 REV 06 DATED 8/01/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
P2	6.5 FT 3W-18GA				LYNN ELEC	LGF3-18-6.5W-MOD	931900101
R1	300-	25W	1%		RCL	AL25-300	210603010

MP MASTER
MA22609

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